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Final Technical Report
May 1979

RELIABILITY EVALUATION OF PROGRAMMABLE READ—ONLY MEMORIES (PROMs) PART III, ULTRAVIOLET ERASABLE PROMs

Hughes Aircraft Company

A. P. Arquero
R. L. Barch
M. B. Colligan
R. L. Long, Jr.

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Ultraviolet erasable programmable read-only memories (UV-PROMs), type 2708 and 8192-bits capacity, were evaluated. Military grade parts were obtained from two manufacturers. All parts were put through screening tests for package hermeticity, erasability, programmability, and electrical performance. A Tektronix S-3260 automatic test system was used for electrical measurements. "Shmoo" plots showed that these UV-PROMs can operate with power supply tolerance of ±10 percent at -55 to +125°C. Retention of data during storage (Cont'd)

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was found to be adequate. No electrical degradation after more than 50 write-erase cycles was detected. At least 30 minutes of exposure to ultraviolet light should be used for erasing. UV lamp calibration procedures were described.

The input protection networks of the UV-PROMs were found to be adequate. Measurements of thermal resistance and input power indicated that junction temperatures are low enough for good reliability. Operating life tests showed that a burn-in duration of 168 hours at 125°C would be adequate. The output disable time appeared to be outside of specifications on nearly all parts at the end of the high temperature tests. This was attributed to a testing problem, not an inherent weakness of the devices, because manual retests did not substantiate the failures.

The recommended procedure for programming the UV-PROMs is to have the product of the number of programming loops and the programming pulse width (in milliseconds) be at least 100 ms, with a pulse amplitude of 26V± 1V. Only two catastrophic failures occurred during this study, both attributed to exceeding 27V during programming. A draft of a MIL-M-38510A detailed specification for 8192-bit UV-PROMs was prepared. Subjects for further investigation were suggested but the results so far indicate that UV-PROMs which meet the draft specification will perform reliably in military applications.

PREFACE

This final report was prepared by Hughes Aircraft Company as part of Contract F30602-75-C-0294, Supplemental Agreements P00007-P00010. The study extended from 13 May 1977 to 13 May 1978 and was sponsored by Rome Air Development Center. James Dobson was the RADC Project Engineer.

The Program Manager for this project at Hughes was R. L. Long, Jr. The individuals responsible for the technical efforts were A. P. Arquero, R. L. Barch, and M. B. Colligan. Among the other Hughes personnel who participated in this study, special acknowledgement is made to J. M. Townsend, who prepared the test programs for the S-3260 test system and performed most of the tests with that equipment, to A. Dolce, who prepared most of the draft specification, and to E. R. Moody, who made the thermal resistance measurements.

Thanks also go to the individuals at Rome Air Development Center, Intel, and Texas Instruments who contributed to this program.

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EVALUATION

The objective of this study was to evaluate and establish effective reliability procedures for testing, qualifying and screening Ultraviolet Erasable Programmable Read-Only Memories, or UV PROMs. This study concentrated on programming and erasing methods, programmability, erasability and functional testing. Short term (1,000 hrs) data retention testing was done at 25°C, 125°C, 150°C and 200°C.

The results of the study and discussions with the vendors were used to determine screening, testing and temperature requirements for the UV PROM. The study is considered successful in meeting the initial objectives established at the beginning of the program.

The major significance of the study is that it provides a background of technical understanding of the problems associated with screening and qualifying UV PROMs. Using the results of the study, the contractor prepared a draft detailed specification for MIL-M-38510, General Specification for Microcircuits.

James J. Dobson
JAMES J. DOBSON
Solid State Applications Section
Reliability Branch

1. INTRODUCTION

1.1 PURPOSE OF STUDY

This final report summarizes the results of a study performed by the Technology Support Division of Hughes Aircraft Company under Rome Air Development Center Contract F30602-75-C-0294, Supplemental Agreements P00007-P00010. The title of this contract is "Reliability Evaluation of Programmable Read Only Memories (PROMs)." The primary goals of the additional tasks of the Supplemental Agreements were:

1. To evaluate and establish reliability procedures for electrical testing, qualifying and screening floating-gate avalanche injection MOS (ultra-violet erasable) programmable read-only memories (UV-PROMs).
2. To prepare a draft of a detailed specification (MIL-M-38510 slash sheet) for UV-PROMs.

1.2 SCOPE

The scope of this effort is limited to 8192 bit UV-PROM devices suitable for high reliability military applications. The specific tasks which were to be accomplished during this phase of the contract are summarized as follows:

Task 1. Device (and Vendor) Selection
- a. Procurement
- b. Screening

Task 2. Electrical Characterization
- a. Programming of S-3260
- b. Testing

Task 3. Special Reliability Evaluations
- a. Data Retention Investigation
- b. Input Protection Networks
- c. Thermal Properties

Task 4. Optimum Procedures Test

a. Develop test plan to include operating life and storage life, both biased and unbiased, output load conditions, test temperatures, data patterns, procedures, and the number of programming-erase cycles.

b. Approval by Contract Officer.

c. Conduct Tests

Task 5. Test Data Analysis

Task 6. Failure Analysis, including recommendations for screens

Task 7. Preparation of Draft Specification

A flow chart of the UV-PROM tests conducted during this study is presented in Figure 1.

1.3 BACKGROUND

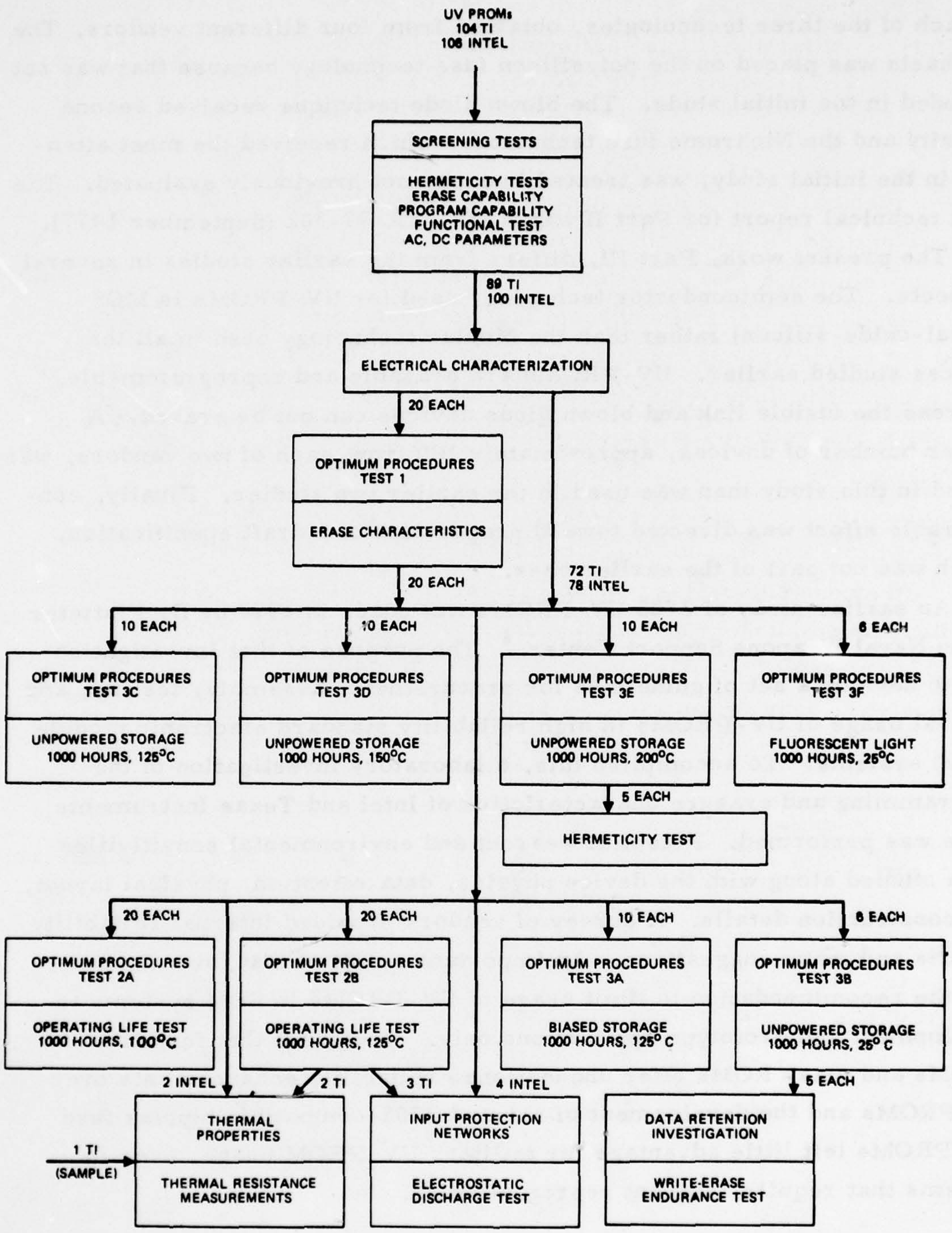
This study is the third in a series of reliability evaluations of PROMs. The objectives of the initial study were to:

- Assess unique factors affecting the reliability of bipolar PROMs employing Nichrome fusible links, titanium-tungsten fusible links, and the avalanche induced migration (blown diode) technique.
- Recommend programming, testing and screening guidelines for the subject PROMs.
- Develop a failure rate prediction technique for the subject PROMs.

The test vehicles used were 1024 bit devices from four different vendors. The final technical report for that study was RADC-TR-75-278 (February 1976).

The objectives of Part II of this series were to:

- Assess factors affecting the reliability of bipolar PROMs employing polycrystalline silicon fusible links, the avalanche induced migration (blown diode) technique, and Nichrome fuse links.
- Investigate programming and associated failure mechanisms.
- Assess the reliability of these PROMs via a life test.


UV PROMs
104 TI
108 INTEL
SCREENING TESTS
HERMETICITY TESTS
ERASE CAPABILITY
PROGRAM CAPABILITY
FUNCTIONAL TEST
AC, DC PARAMETERS
89 TI
100 INTEL
ELECTRICAL CHARACTERIZATION
20 EACH
OPTIMUM PROCEDURES
TEST 1
ERASE CHARACTERISTICS
20 EACH
72 TI
78 INTEL
10 EACH
10 EACH
10 EACH
6 EACH
OPTIMUM PROCEDURES
TEST 3C
UNPOWERED STORAGE
1000 HOURS, 125°C
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1000 HOURS, 200°C
OPTIMUM PROCEDURES
TEST 3F
FLUORESCENT LIGHT
1000 HOURS, 25°C
5 EACH
HERMETICITY TEST
20 EACH
20 EACH
10 EACH
6 EACH
OPTIMUM PROCEDURES
TEST 2A
OPERATING LIFE TEST
1000 HOURS, 100°C
OPTIMUM PROCEDURES
TEST 2B
OPERATING LIFE TEST
1000 HOURS, 125°C
OPTIMUM PROCEDURES
TEST 3A
BIASED STORAGE
1000 HOURS, 125° C
OPTIMUM PROCEDURES
TEST 3B
UNPOWERED STORAGE
1000 HOURS, 25° C
2 INTEL
2 TI
3 TI
4 INTEL
5 EACH
1 TI
(SAMPLE)
THERMAL
PROPERTIES
THERMAL RESISTANCE
MEASUREMENTS
INPUT PROTECTION
NETWORKS
ELECTROSTATIC
DISCHARGE TEST
DATA RETENTION
INVESTIGATION
WRITE-ERASE
ENDURANCE TEST

Figure 1. Reliability evaluation of ultraviolet erasable PROMs.

The test vehicles for this study were 1024, 2048, and 4096 bit devices of each of the three technologies, obtained from four different vendors. The emphasis was placed on the polysilicon fuse technology because that was not included in the initial study. The blown diode technique received second priority and the Nichrome fuse technology, which received the most attention in the initial study, was treated in areas not previously evaluated. The final technical report for Part II was RADC-TR-77-302 (September 1977).

The present work, Part III, differs from the earlier studies in several respects. The semiconductor technology used for UV-PROMs is MOS (metal-oxide-silicon) rather than the bipolar technology used in all the devices studied earlier. UV-PROMs are erasable and reprogrammable, whereas the fusible link and blown diode devices can not be erased. A larger number of devices, approximately 100 from each of two vendors, was tested in this study than was used in the earlier two studies. Finally, considerable effort was directed toward preparation of a draft specification, which was not part of the earlier ones.

An earlier study of 2708 UV-PROMs was made in 1977 by D. Platteter at the Naval Weapons Support Center.[1] The purpose of that investigation was to develop a set of guidelines for procurement, assembly, testing, and general usage of UV-PROMs in high reliability standard electronic module (SEM) systems. To accomplish this, a laboratory investigation of the programming and erasure characteristics of Intel and Texas Instruments parts was performed. Potential wearout and environmental sensitivities were studied along with the device physics, data retention, physical layout, and construction details. A survey of vendors provided internal reliability reports and many suggestions. An important result of that investigation was the recommendation to limit usage of UV-PROMs in SEM systems to development and prototype applications only. It was felt that fuse link PROMs and mask ROMs offer unquestioned reliability enhancements over UV-PROMs and the development of several 2708-compatible bipolar fuse link PROMs left little advantage for military UV-PROM usage, even in systems that require frequent reprogramming.

1.4 UV-PROM TECHNOLOGY DESCRIPTION

The UV-PROM technology[2] is based on the floating gate avalanche injection MOS transistor.[3] This is a MOS field effect transistor in which no connection is made to the silicon gate. To program the transistor, which is one cell of the memory, charge is injected onto the gate by avalanches of high energy electrons from the source or drain regions of the transistor. The injected charge offsets the threshold voltage of the transistor, as determined by a second silicon gate (the select gate) on top of the floating gate. (The two gates are separated by a layer of silicon dioxide.) Erasure of the memory is effected by exposing the device to ultraviolet light, which produces a photocurrent in the oxide that discharges the floating gate. Therefore the UV-PROM package incorporates an ultraviolet-transmitting quartz window over the chip.

The UV-PROMs investigated in this study were 8,192 bit devices, organized as 1,024 eight bit words. This size UV-PROM and larger ones are n-channel MOS devices. Photographs of the Intel MC2708 chip and the Texas Instruments SMJ2708 chip, which are used in this study, are shown in Figures 2 and 3. Although the chips are nearly the same size, have the same pin-outs and are electrically compatible, the circuit layouts on the chips are significantly different. (The 8K UV-PROM currently supplied by Texas Instruments is different from that shown in Figure 3, since the die size has been changed and double doping of the polysilicon interconnections is now used.)

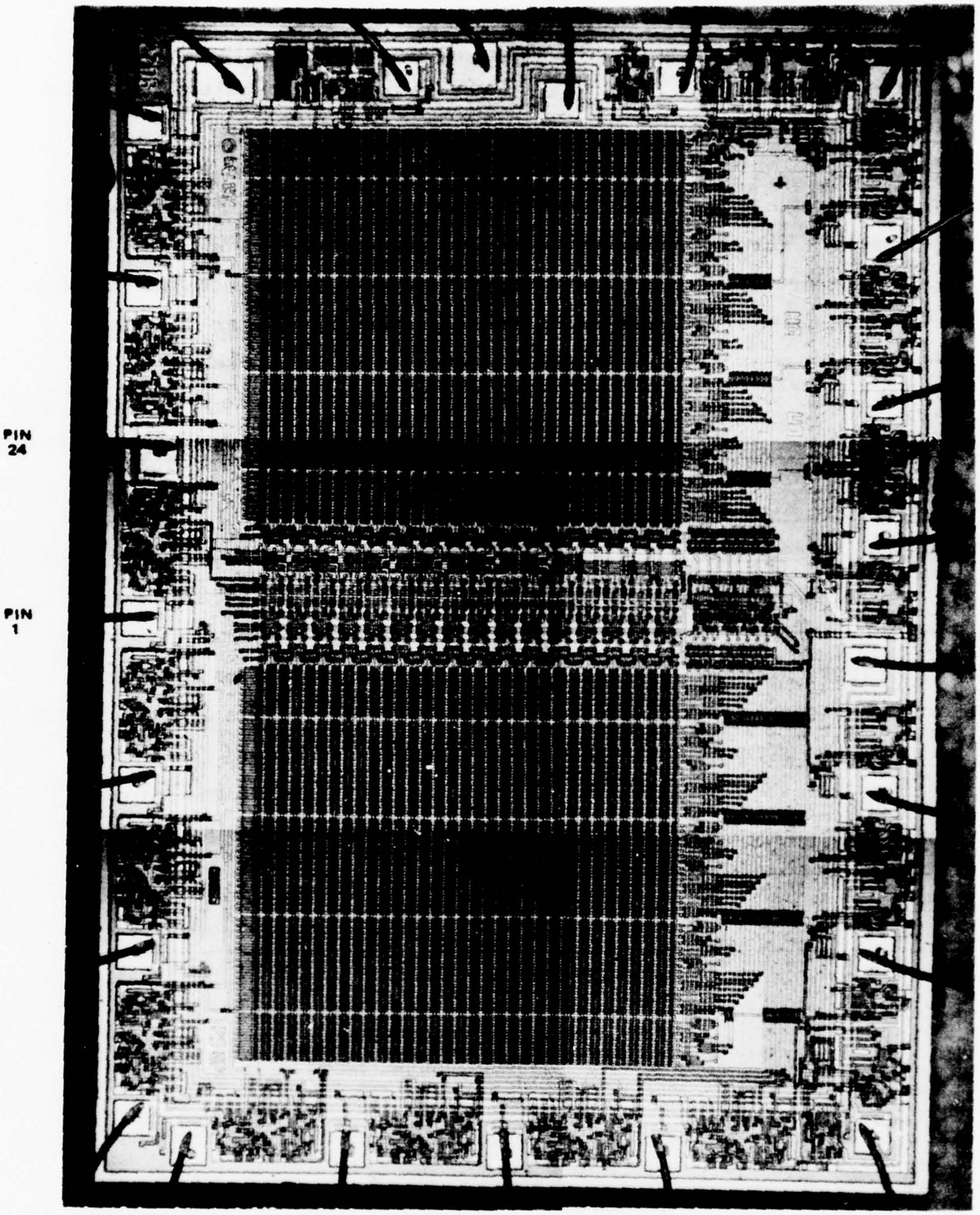


Figure 2. Intel's UV-PROM chip, MC2708. The actual chip size is 0.135 x 0.188 inch.

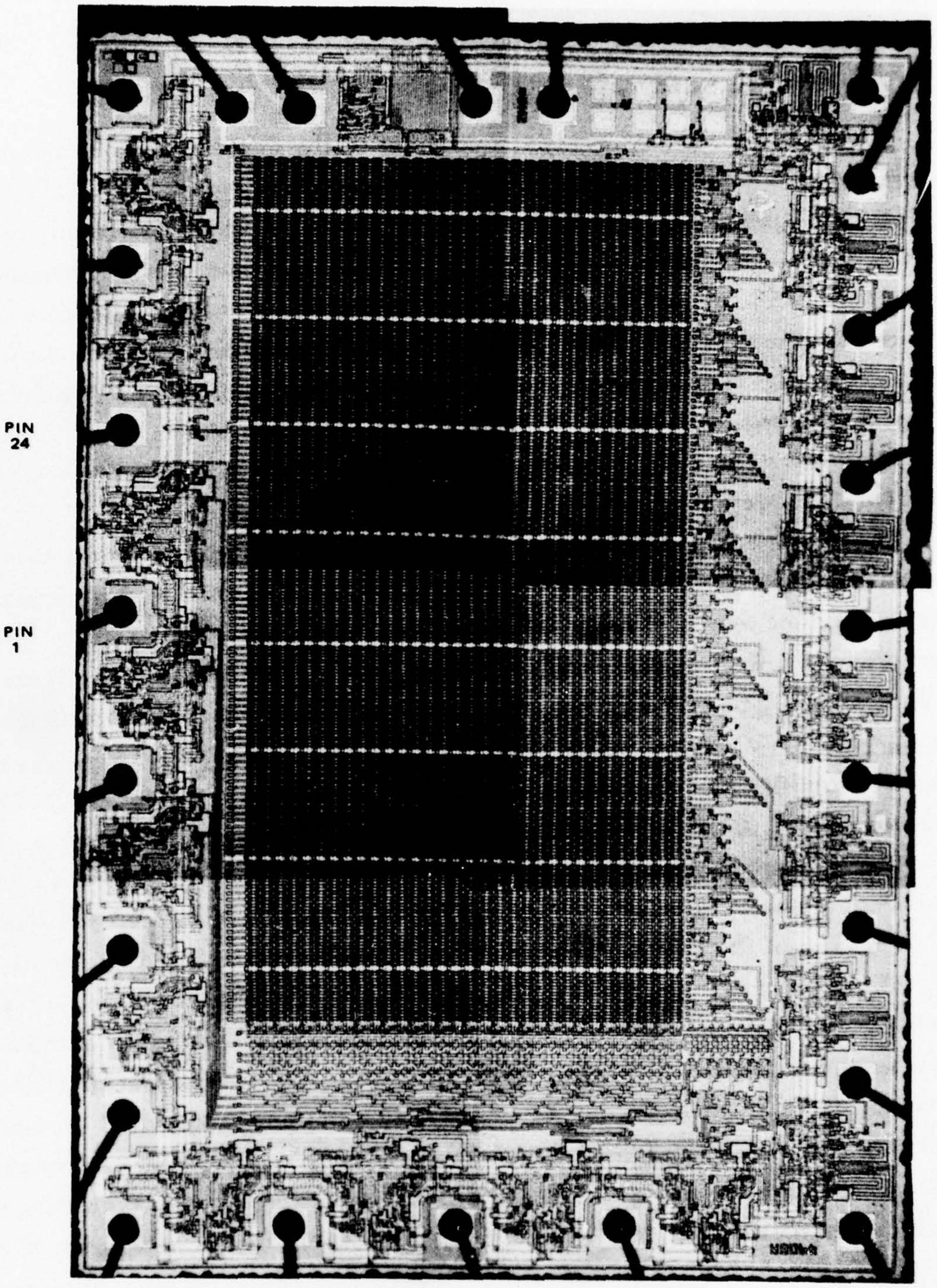


Figure 3. Texas Instrument's UV-PROM chip, SMJ2708.
The actual chip size is 0.190 x 0.125 inch.

2. DEVICE SELECTION

2.1 CHOICE OF SUPPLIERS

When the UV-PROM study amendment to the contract was proposed in January 1977, only commercial grade (temperature range 0 to +70°C) type 2708 UV-PROMs (8192-bit) were available from Intel and AMS (now Intersil). By the start of the procurement cycle, it appeared that military temperature range (-55 to +125°C) type 2708 parts would be available from four or five manufacturers but at considerably higher cost than had been estimated for the commercial grade product. Based on this information, military temperature range 8192-bit parts from additional suppliers were to be substituted for the 2048-bit parts listed in the original proposal (per Supplemental Agreement P00009).

Intel designed and developed the first 2708's and was the first to market the military temperature range product. Because of this lead in experience, Intel's product was obviously the prime candidate for investigation. Texas Instruments' military temperature range 2708's first became available in July 1977. Thus TI was the first of the major MIL qualified semiconductor manufacturers to commit itself to production of a military grade product. This plus TI's qualification to supply many other digital IC's to MIL-M-38510 was a major factor in the selection of TI as the second supplier for parts.

The increased cost of the military temperature range parts over that of the commercial temperature range parts originally budgeted precluded the purchase of the 100 parts needed for characterization and life tests from more than two suppliers. An attempt was made with the remaining funds for parts to purchase as many electrical characterization samples from as many additional suppliers as possible. The results of this attempt were not entirely satisfactory as Intersil was the only additional vendor able to supply military temperature range 2708's. The other LSI manufacturers "NO BID" our purchase order for military temperature range product, indicated that they did not intend to build any, or would not have it available in time for inclusion in this program. These manufacturers were Electronic Arrays Inc., Fairchild Semiconductor, Mostek, Motorola, National Semiconductor, and Signetics.

Since the fall of 1977, the market situation has continued to change. Intersil has ceased manufacturing 2708's altogether. Motorola, Fairchild, and AMD have announced "off-the-shelf" availability of military-temperature range 2708's. National and Signetics are working on military-temperature range parts and expect to have them available by the third quarter of 1978. Mostek is producing commercial grade 2708's in quantity but is not planning to develop a full temperature range version.

A list of the UV-PROMs obtained for this study is given in Table 1. All the screened and -55 to 100/125°C parts were in alumina ceramic dual in-line packages with side brazed leads and a quartz window on top. The Texas Instruments (TI) packages were black ceramic and the Intel parts were white ceramic. An analysis of the two different color ceramic packages by energy dispersive analysis of x-rays on a scanning electron microscope did not reveal any significant difference in composition.

TABLE 1. UV-PROM SAMPLES RECEIVED

Vendor	Part No.	Date Code	Serial Numbers	Additional Information
Intersil	AMS7708		1, 2	Samples, 0 to 85°C
Intersil	MH2708		500-505	-55 to 125°C
TI	TMS2708JL	7713	10-13	Samples, 0 to 85°C
TI	SMJ2708JM	7739	15-74	Screened, vendor equiv. 883 level B
TI	TMS2708JM	7741	75-114	-55 to 125°C
Intel	MC2708	7717	300-326, 328-330	-55 to 100°C
Intel	MC2708	7716	327	-55 to 100°C
Intel	MC2708/B	7727	331-395	Screened, vendor equiv. 883 level B
Intel	MC8708	7717	400-409	-55 to 100°C

2.2 SCREENING

All of the UV-PROMs received from Intel and Texas Instruments were processed through a series of tests to establish package integrity, erasability, programmability, and electrical performance, as shown in Figure 1. A summary of the results of these tests appears in Table 2.

Package Hermeticity

The devices were tested for package integrity with fine and gross leak tests in accordance with MIL-STD-883, Method 1014.2, conditions B and C. All devices were serialized after the hermeticity tests.

Since the UV-PROM package has the unusual feature of a quartz window on its top lid, package hermeticity was of particular interest. Therefore the gross and fine leak tests were repeated near the end of this study on five parts from each of Intel and TI. The parts retested were those that had been used for the 200°C storage test, Optimum Procedures Test 3E (see section 5), programming method P1. They had been at 200°C for 1000 hours with five interruptions for testing at temperatures of -55, 25, 100 and 125°C. Before that test, they each had been tested more than twice at the same four temperatures. All ten devices passed the second gross and fine leak tests. Therefore no problems with the quartz window seals were detected in this program and they are not expected to affect the reliability of UV-PROMs.

Erasability

All devices were exposed to ultraviolet light for a minimum of 20 minutes to erase them prior to any electrical testing. A model S-52T UV lamp, manufactured by Ultraviolet Products, Inc., was used as the light source. After the initial exposure of 20 minutes, each device was read (in a functional test on the Tektronix S-3260 automated tester) to determine if all cells were in the erased or unprogrammed state. Any failure at this point required an additional 20 minute erase cycle. If the device successfully completed the functional test, all input currents, output voltages, output leakage currents, and all power supply currents were tested to the manufacturer's specification at 25°C.

TABLE 2. SCREENING TEST RESULTS, USING VENDOR SPECIFICATIONS FOR MILITARY PARTS

Manufacturer		Intel		Intersil		Texas Instruments	
Part Number		MC2708, MC8708		AMS7708, MH2708		TMS2708, SMJ2708	
Quantity Received		106		8		104	
Labeled		300-395, 400-409		1[a], 2[a], 500-505		10-13[a], 15-114	
SCREENING TESTS		Pass	Fail	Pass	Fail	Pass	Fail
Hermeticity	Fine	105	1	6[b]	0	103	1
	Gross	105	1	6	0	99	4
Erase Capability		104	1	6	0	94[b]	0
Program Capability		104	1[c]	6[d]	0	94	0
Functional		103	0	1	4	94	0
AC, DC Parameters		100	3[e]	0	5[e]	89	5[f]

Notes:

a. Set-up samples.

b. Set-up samples and parts (numbers 74 and 62) with some missing pins were not processed further.

c. Not the same part that failed the erase capability test.

d. SN 500 was damaged during programming characterization and not processed further.

e. None were screened by vendor.

f. All were screened by vendor.

Of the devices tested, only Intel parts have exhibited erasure difficulties. One device (SN305) has failed to erase on all attempts. Two devices (SN306 and 402) initially required two twenty minute erase cycles. However, all further erase attempts were successful after only one twenty minute exposure One device (SN401) has consistently required two twenty minute cycles to completely erase it.

Programmability

All devices which passed the erase test and the DC parameter checks were subjected to a sequence of program and erase cycles to ascertain the programmability of each cell of the device. The assumption at this point was that the device was indeed functional and each cell could be addressed. The devices were first programmed to a row-column checkerboard, then read to check that the appropriate locations were either programmed or not programmed. The devices were then erased, reprogrammed to the inverse of the original pattern, and read a second time to verify each cell's status. As is the case in most row-column checkerboard patterns, the actual programmed pattern turns out to be alternating columns of 1's and 0's through most of the memory. This was verified by computer simulation of this pattern in a vendor-supplied bit map. Since the purposes of this test are to eliminate devices with programming problems and to catch faults such as cells that are stuck at one or stuck at zero and shorts between cells, a true checkerboard pattern based upon the physical bit map would be more useful. For this reason, vendors' bit maps (see Appendix C) were obtained and checkerboard, when implemented, was based upon these maps thereafter.

Electrical Performance

Each device that passed the programmability test was erased and reprogrammed for the electrical performance tests. It would be desirable to program the UV-PROMs with a pattern that would be unique for each of the 2^{10} words in the device in order to detect decoder errors, but that is impossible with only the 8 bits per word that are available. The program chosen was a binary count pattern, in which the data stored in each word are the eight least significant address bits for that word. This pattern was chosen for its ease of implementation. Since the pattern repeats only four times within the memory, the chance of catching decoder errors is significantly higher than if a checkerboard pattern were used.

After programming the devices with the binary count pattern, they were subjected to functional, AC and DC parametric tests, done over the full military temperature and voltage ranges. These tests were originally performed with all power supply voltages at three different levels: nominal, nominal +10 percent, and nominal -10 percent. The tests were later modified, as discussed below, to cover five supply voltage conditions, including both ±5 percent (Texas Instruments) and ±10 percent (Intel) specifications.

The initial test results, as reported in the Interim Report for this program, indicated high failure rates for the Intel, TI, and Intersil devices. (See Appendix E.) Subsequent investigation showed that three factors contributed to that erroneously pessimistic evaluation:

1. The programming procedure: Only as many programming loops were used as was necessary for the device to verify at nominal supply voltages and room temperature. Although this method was successful for the first parts received from Intel and TI and it required the minimum time, it resulted in marginally programmed devices.
2. The pass-fail criteria used were incorrect: The parameters for commercial temperature range (0-70°C) parts were used instead of those for the military temperature range (-55°C to 125°C). The latter are less restrictive than the former.
3. The vendors' specifications differ: Differences exist in voltage margins, timing, and temperature ranges.

Therefore all parts were erased and reprogrammed according to method P1, which is described on Page 38. This method uses the minimum number of programming loops necessary to verify at nominal voltages and room temperature (as before) and then do eighty additional loops. A 0.5 ms programming pulse width was used here, as in all the routine programming done on the S-3260. The parts were then retested and evaluated against the proper vendor specifications, which are listed in Table 3. The results, summarized in Table 2, were much

TABLE 3. SCREENING TEST LIMITS FOR MILITARY GRADE UV-PROMS

	Vendor	
Parameter	Intel	TI
t_{ACC}	450 ns	450 ns
$t_{\overline{CO}}$	120 ns	160 ns
t_{DF}	120 ns	160 ns
t_{OH}	0	0
I_{LI}	10 μA	10 μA
I_{LO}	10 μA	10 μA
I_{DD}	80 mA	50 mA
I_{CC}	15 mA	8 mA
I_{BB}	60 mA	25 mA
V_{OL}	0.45V	0.45V
V_{OH1}	3.7V	3.7V
V_{OH2}	2.4V	2.4V
V_{BB}	-5V ±10 percent	-5V ±5 percent
V_{CC}	5V ±10 percent	5V ±5 percent
V_{DD}	12V ±10 percent	12V ±5 percent

better and quite normal for MOS devices. However, all five remaining Intersil parts still failed, so they were excluded from subsequent testing. Of the 197 Intel and TI parts tested for electrical performance, 95 percent met the vendors' specifications even over the full temperature range (the nominal limit for the Intel parts is 100^{o} C) and at the normal military power supply limits of nominal + 10 percent. (The TI specification is ± 5 percent and a total of 7 TI parts failed to meet the wider specification.) A more detailed summary of these results is presented in Appendix A.

The results of all the screening tests, neglecting the eight Intersil and the four sample TI parts, show an overall yield of 189 out of 206 parts, or 92 percent (see Table 2). Four of the five TI parts which did not meet all TI specifications in the AC and DC parameters test were included in some of the subsequent tests in order to have a suitable number of samples. The parts not used in the subsequent tests are listed in Table 4.

TABLE 4. UV PROMs NOT USED FOR TESTS

Serial Number	Vendor	Reason
1, 2	Intersil	Samples, not military grade
10-13	TI	Samples, not military grade
11	TI	Failure Analysis - High current on programming pin; sub-oxide arc-over
33	TI	Failed AC/DC Screening
62	TI	Missing Pin
70-73	TI	Failed Hermeticity
74	TI	Missing Pin
301	Intel	Failed AC/DC Screening
305	Intel	Failed to Erase
306	Intel	Failed AC/DC Screening
317	Intel	Failed AC/DC Screening
395	Intel	Failed Hermeticity
402	Intel	Failed to Program
500	Intersil	Failure Analysis - Reported programming pin overstressed; sub-oxide arc-over
501-505	Intersil	Failed AC/DC Screening

3. ELECTRICAL CHARACTERIZATION

UV-PROMs from each vendor were subjected to a series of characterization tests to verify the vendors' specifications or to determine unspecified minimum and maximum DC, AC and functional parameters for which the devices would operate over the -55°C to +125°C temperature range. All testing was accomplished on a Tektronix S-3260 automatic IC test system utilizing accepted techniques for testing individual parameters. Any deviations from standard techniques are described in detail in the appropriate test description.

3.1 S-3260 TEST PROGRAMS

All the S-3260 programs generated for this study follow a format established by the Technology Support Division of Hughes Aircraft Company. Each program contains sufficient labels to identify the particular test and the conditions under which the test was performed. This programming technique has eliminated the need for flow diagrams to document a given test program. Other S-3260 users, in general, have little trouble following the flow of a program. Users of other types of automatic test systems have, in the past, been able to absorb enough information from program listings in this format because of the modularity of the programming technique and the English language syntax of the test software.

Receiving Test

This is the basic S-3260 test program and includes the functional tests, AC parametric measurements and DC parametric measurements used in screening (see Section 2). The functional test consists of three tests done under nominal timing and minimum, nominal, and maximum supply voltage conditions. Its purpose is to ensure that the device has been programmed with the proper pattern and that it reads at the minimum and maximum voltage conditions. If a device fails, the program provides the first address which fails as well as the output which failed. The AC and DC parametric measurements are made utilizing techniques described in Section 3.2. All limits and conditions used were those specified in the manufacturers' data sheets (see Table 3).

Characterization Tests

These programs are specialized versions of the basic receiving test but no pass or fail condition is sought. Because of the unique capability of having temperature as well as all other test parameters controlled by the system computer, all data was accumulated by the computer and tabulated or plotted at a later date. Examples are shown in Appendices D and E.

Programming

The device requirement of a specified rise-fall time on the programming pulse required that an external driver be designed for the Tektronix S-3260 automated test system. The circuit shown in Figure 4 was fabricated to program all UV-PROMs on the S-3260. The following procedure was used: (a) Appropriate voltages were applied to the device and one programming loop performed. (b) The 1803 Test Station of the S-3260 was initialized, appropriate conditions set, and a functional test was performed. If the device failed to program, the power was removed from the device and the S-3260 program was returned to step (a). If the device was properly programmed, the programming sequence was stopped and the number of programming loops recorded.

During the course of the study three programming algorithms were tried. (Pulse widths of 0.5 ms were used in all three cases.) The initial algorithm consisted of applying one program loop (where one program loop is a complete sequence through all addresses, 0-1023), then reading the device to check if its contents matched the desired pattern. The process was repeated until the device did verify. Typically the device would verify in 20 or less program loops. A few devices, especially those from Texas Instruments, would verify after only one program loop.

Because of the high failure rate due to marginally programmed cells, as discussed in Section 2.2, a second S-3260 programming algorithm was implemented. This algorithm is shown on Page 38 as programming Method P1.

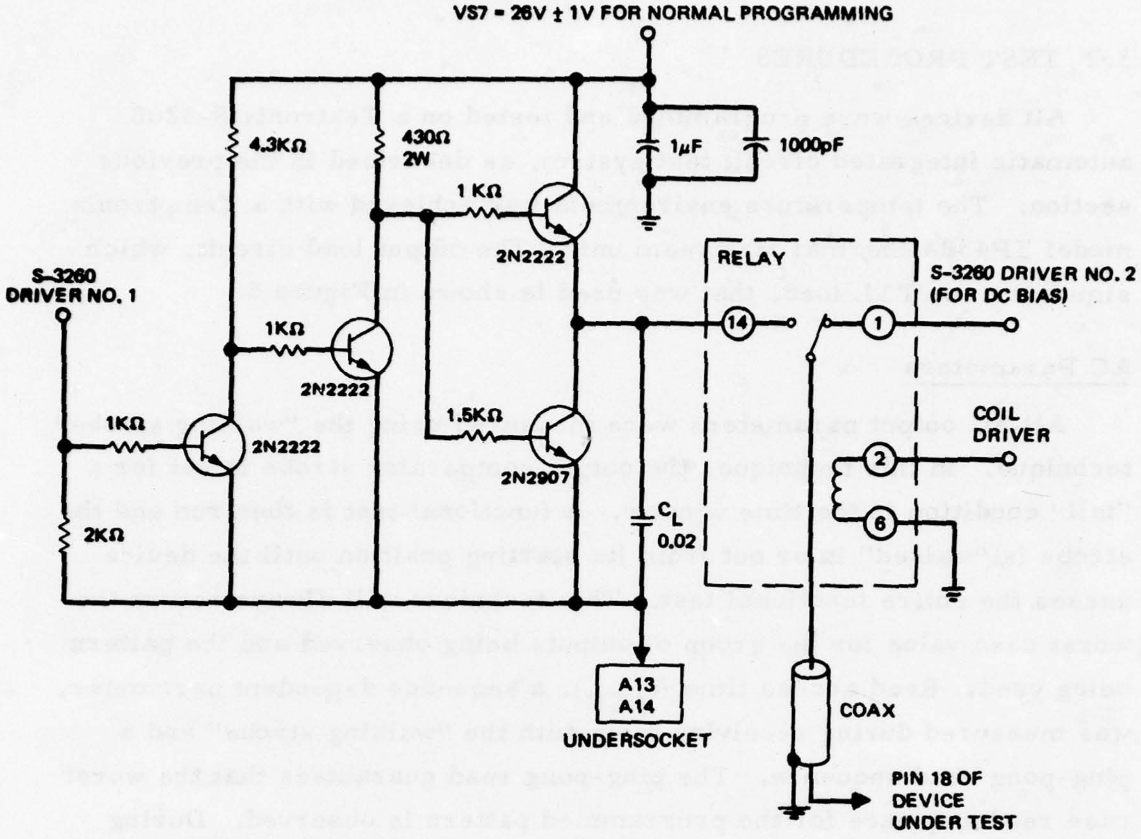

VS7 = 26V ± 1V FOR NORMAL PROGRAMMING
4.3KΩ
430Ω
2W
1μF
1000pF
1 KΩ
2N2222
RELAY
S-3260
DRIVER NO. 1
S-3260 DRIVER NO. 2
(FOR DC BIAS)
1KΩ
2N2222
14
1
1.5KΩ
COIL
DRIVER
1KΩ
2N2222
2N2907
2
6
2KΩ
C
L
0.02
A13
A14
UNDERSOCKET
COAX
PIN 18 OF
DEVICE
UNDER TEST

Figure 4. Driver circuit for programming UV-PROMs on the S-3260.

The second algorithm performs a program and verify cycle sequence until the device verifies, then the device is programmed further for 80 more programming loops. Utilizing this method, the failure rate was reduced significantly, as discussed previously.

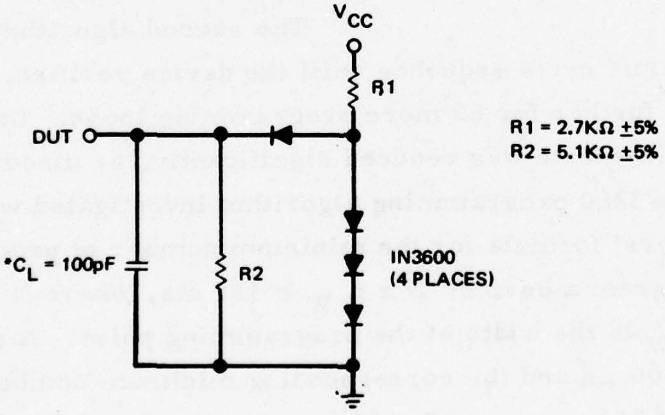
The third S-3260 programming algorithm investigated was based upon the manufacturers' formula for the minimum number of programming loops required to program a device: $N \times t_{PW} \geq 100$ ms, where N is the number of loops and t_{PW} is the width of the programming pulse. A programming pulse width of 500 μs and the corresponding minimum number of programming loops, N = 200, were used. This programming method was utilized only during the Optimum Procedures Tests to investigate any possible differences between it and the second algorithm (minimum plus 80).

3.2 TEST PROCEDURES

All devices were programmed and tested on a Tektronix S-3260 automatic integrated circuit test system, as described in the previous section. The temperature environment was achieved with a Temptronix model TP450A thermal airstream unit. The output load circuit, which simulates one TTL load, that was used is shown in Figure 5.

AC Parameters

All AC output parameters were measured using the "walking strobe" technique. In this technique, the output comparator strobe is set for a "fail" condition in the time window. A functional test is then run and the strobe is "walked" in or out from its starting position until the device passes the entire functional test. This technique will always return the worst case value for the group of outputs being observed and the pattern being used. Read access time (t_{ACC}), a sequence dependent parameter, was measured during receiving tests with the "walking strobe" and a ping-pong read sequence. The ping-pong read guarantees that the worst case read sequence for the programmed pattern is observed. During characterization tests, in order to minimize test times, a simple scan-read was used to plot the variations in t_{ACC} with temperature and supply



* C_L IS THE TOTAL CAPACITANCE PRESENTED TO THE DEVICE UNDER TEST (DUT).

Figure 5. Simulated TTL load circuit.

voltages. An example is shown in Appendix D. Since display of parameter deviations under varying conditions is the intent of plots, the absolute worst case measurement was not considered necessary.

The remainder of the AC parameters, $t_{\overline{CO}}$, t_{DF}, and t_{OH}, were measured with a simple scan read pattern. t_{DF} (output disable time) was the most difficult of the parameters to obtain correlation on because of its dependence upon the capacitance which the measurement system presents to the device. A second problem is the reference level on the output waveform, which is discussed in Section 3.3 (see Figure 6). Although no pass or fail criterion is assigned for t_{DF}, the technique employed is an accepted one for use on automated test systems and is a method accepted by manufacturers of bipolar tri-state devices. For characterization purposes, it yields usable and repeatable measurements.

DC Parameters

All DC input and output parameters were tested in accordance with MIL-STD-883 methods, using the limits and forcing functions specified by the manufacturers. All output parameters (V_{OL}, V_{OH1}, V_{OH2}, and I_{LO}) were measured utilizing a search routine which finds the first available test vector at which the output is in the proper state. This technique allows the same test program to be used for all UV-PROMs with no dependence upon the specific pattern programmed into the device. The only requirement

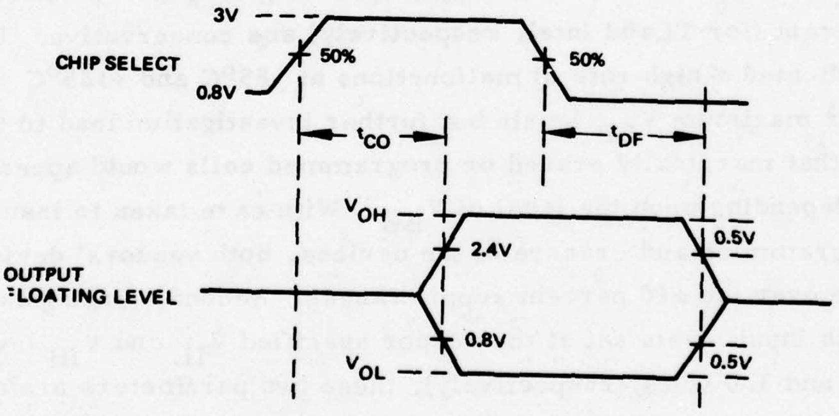


Figure 6. Switching time reference levels for t_{DF}.

is that each output be high and low at least once in the test pattern. All input current tests require no preconditioning of the device. Each measurement is taken independently with a current auto-ranging routine to ensure that all devices, good or bad, can be measured with maximum resolution. The power drain current measurements (I_{DD}, I_{BB}, and I_{CC}) are also measured statically with automatic ranging. An example plot of the I_{DD} data is shown in Appendix D.

3.3 RESULTS

Worst Case Input and Power Supply Voltages

The device operating region for vendor specified input low and high thresholds was determined by plotting device functionality as a function of the three power supplies. (The resulting plots are called shmoo plots; see Appendix E.) For convenience, the term 'operational' was taken to mean that the stored pattern was able to be read at all addresses with the strobe set at 1 μs, well beyond the limits of all timing parameters. The only stipulation was that logic output levels would meet the 0.45 volt maximum for logic zero and the 3.7V minimum for a logic one under the single TTL gate load specified for dynamic tests. Any failure to meet this criterion was considered a non-operational state.

The series of shmoo plots for temperatures of -55, +25, +100, and +125°C accomplished three things. First, they showed that for the devices tested the vendor specified power supply operating ranges of ±5 percent and ±10 percent (for TI and Intel, respectively) are conservative. Initial data had indicated a high rate of malfunctions at -55°C and +125°C at minimum or maximum V_{BB} levels but further investigation lead to the conclusion that marginally erased or programmed cells would appear or disappear depending upon the level of V_{BB}. With care taken to insure proper programming and erasure of the devices, both vendors' devices will operate over the ±10 percent supply ranges. Second, since this test was run with input levels set at the vendor specified V_{IL} and V_{IH} levels (0.65 volts and 3.0 volts, respectively), these two parameters are also verified for the voltage and temperature range. Third, device noise margins and V_{BB} margins, although not investigated as distinct parameters, are guaranteed by the observed performance of the device over the wide supply voltage ranges studied. Since the device is non-dynamic in nature (i.e., data and addresses are non-clocked functions), the static test results are adequate to verify these margins.

Worst Case Read Characteristics

As in any memory device, the sequence in which a device is read is the determining factor in finding worst case read access time. The limiting factor in any such measurement is the speed of operation of the address decoder/multiplexer of the device. A full check of the effects of address sequence can be accomplished with the so-called "ping-pong" (or galloping) read. Since each address precedes or follows every other address during this sequence, the effect of sequence can easily be studied. As suspected, the ping-pong read did produce the largest readings for access time. However, the typical difference between access time measured with a ping-pong pattern and a scan pattern is only 10-15 ns, less than a 10 percent difference in a typical reading. (The scan pattern utilized here is a simple read sequence from address 0 through address 1023.) A considerable savings in test time can be achieved if a ping-pong read is replaced with a scan read. All that would be required is an appropriate adjustment in test limits to validate any results obtained.

A similar study for pattern sensitivity was performed for each of the other AC parameters. $t_{\overline{CO}}$ (chip select to output delay), t_{DF} (chip de-select to output float), and t_{OH} (address to output hold) were all examined for variations due to pattern read sequence and stored pattern. As in the case of t_{ACC} (address access time), each device was tested with a checkerboard, an inverse checkerboard, and a count pattern. In all cases, the AC parameters were essentially independent of stored pattern. $t_{\overline{CO}}$ and t_{DF}, as suspected, are independent of read sequence or address but they do depend upon load and power conditions. Utilizing the Intel guideline of 0.8 V and 2.8 V for input reference levels and 0.8 volt and 2.4 V for output reference levels produced erroneous results during initial efforts. The vendor's choice of phrasing for output load conditions, "1 TTL gate and C_L = 100 pF," leaves some room for interpretation: Is the load a "typical" TTL gate, a worst case TTL gate, a gate simulating passive load, or a gate simulating active load? The standard test practice used was to simulate the current drain characteristics of one TTL gate with a passive network (see Figure 5). To eliminate the problems inherent with the resultant RC network, the V_{OH}, V_{OL} and floating voltage of the output with the load connected were measured. From the resultant voltage levels new reference levels were calculated by adding or subtracting 0.5 volt. The waveforms in Figure 6 illustrate this concept. Utilizing this reference technique standardizes the method of measurement as long as the load is clearly defined. (A similar standard is utilized for bipolar digital devices with tri-state outputs.)

Address to output hold time (t_{OH}) is, in essence, the reverse of access time (t_{ACC}). t_{OH} is a measure of the fastest cell in the matrix. The 0 ns minimum specified by the vendor is misleading because it can only occur if the next address in the sequence contains the same data. A more meaningful measurement is to insure that the next address always contains complement data. Utilizing a simple scan read with a checkerboard stored pattern meets all the requirements. The readings obtained thus represent a more valid picture of the fastest cells in the memory.

Programming Characterization

This study examined the effects of programming pulse width and amplitude on the number of loops required to program the UV-PROMs. The samples used were one TI part (SN12), four Intel parts (SN301, 302, 401, 403) and one Intersil part (SN500). In order to save time, the devices were checked for verification after each of the first several loops and then after every 5 or 10 subsequent loops, so the number of loops recorded (N*) was greater than or equal to the actual number of loops required.

According to the vendors, the number of programming loops (N) and the programming pulse width (t_{PW}) should be chosen so that $Nt_{PW} \geq 100$ ms. For example, if the pulse width is 0.5 ms, at least 200 programming loops should be used. In order to evaluate this criterion, the product of the maximum number of loops and the pulse width used was calculated for each part at each voltage used. The results are presented in Table 5. The maximum value of N^*t_{PW} observed at the nominal programming pulse amplitude of 26V was 31.5 ms, for SN401 at t_{PW} = 0.7 ms (N^* = 40 to 45 loops). At the specification lower limit of 25 V, the maximum value observed was 70. Therefore the vendors' recommendation, $Nt_{PW} \geqq 100$ ms, appears to be a safe criterion for pulse widths of from 0.1 to 0.9 ms.

The TI parts were consistently faster to program than the Intel parts. The number of loops required for the Intel parts varied by a factor of four or more (see Table 5). (One Intel part, SN402, was the only device received which failed to program.) Programming of the Intersil part was similar to the faster two Intel parts. Note that N^*t_{PW} is approximately independent of pulse width for each part so changing t_{PW} will not change the programming time required, since the minimum number of loops required will change proportionately. (This would be expected since the amount of charge injected onto the floating gates of the memory transistors should be proportional to the total time that the programming pulse is applied.)

The programming pulse amplitude upper limit of 27 V appears to be reasonable since one part (Intersil SN500) was damaged in tests at 28 V while no problems were encountered at 27 V. The averages of N^*t_{PW} at 27 V are 60 percent of those at 26 V (except for the TI part, which usually required only one pulse at all amplitudes). Therefore the minimum programming time required could be reduced 40 percent by using 27 V programming pulses. However, there would then be a risk of damaging parts as a result of fluctuation in the pulse amplitude and variation in part tolerances. The programming pulse amplitude lower limit of 25 V is reasonable since the Nt_{PW} product will certainly be greater than 100 ms for amplitudes less than 25 V, which would cause difficulties unless the Nt_{PW} criterion ($\geq$100 ms) were increased.

For the Data I/O programmer, the programming pulse width used is 1 ms and parts requiring more than 128 loops ($Nt_{PW} > 128$ ms) are rejected. The data in Table 5 indicate that criterion should not result in rejection of a significant fraction of parts.

TABLE 5. PROGRAMMING CHARACTERIZATION TEST RESULTS

(Number of loops recorded) x (pulse width) = N*t_{PW} (ms)

t_{PW} (ms)	SN12	SN301	SN302	SN401	SN403	SN500
Programming pulse amplitude = 25 V						
0.1	0.1	7.1	6.1	62.1	24.1	7.1
0.3	0.3	6.3	6.3	63.3	24.3	6.3
0.5	0.5	8	0.5	65.5	25.5	8.0
0.7	0.7	7	6.3	70	23.1	7.0
0.9	0.9	8.1	7.2	58.5	22.4	7.2
Average	0.5	7.3	5.3	64	24	7.1
Programming pulse amplitude = 26 V						
0.1	0.5	4	4	16	15.5	3.5
0.3	1.5	6	4.5	21	16.5	4.5
0.5	0.5	5	5	25	17.5	5.0
0.7	0.7	7	7	31.5	17.5	3.5
0.9	0.9	5.4	4.5	29.7	17.1	3.6
Average	.82	5.5	5.0	25	17	4.0
Programming pulse amplitude = 27 V						
0.1	0.1	2.6	2.1	14.1	9.1	2.1
0.3	0.3	3.3	3.3	15.3	10.8	3.3
0.5	0.5	3	3	15.5	10.5	2.0
0.7	0.7	3.5	2.8	14.7	11.2	2.1
0.9	0.9	3.6	3.6	18.9	9.9	2.7
Average	0.5	3.2	3.0	16	10.3	2.4
Programming pulse amplitude = 28 V						
0.9	0.9	9.9	2.7	-	5.4	-

4. SPECIAL RELIABILITY EVALUATIONS

4.1 DATA RETENTION INVESTIGATION

UV-PROMs, unlike the fuse link and blown diode PROMs studied previously, can be erased and reprogrammed. Therefore particular attention in this study was directed toward the ability of UV-PROMs to retain correct data. Among the avenues of investigation were data retention during storage at elevated temperatures, the effect of repeated write-erase cycles, and the influence of ambient light. Calibration of the UV lamp used for erasing will also be discussed in this section.

Data Retention During Storage

The long term decay rate of data stored in UV-PROMs was investigated in Optimum Procedures Test 3, described in Section 5.3. That test involved biased storage at 125°C, unpowered storage at 25, 125, 150, and 200°C, and exposure to fluorescent light at room temperature. The loss of data in that test was evidenced by failure of the functional (readout) test.

One of the programming methods used (P1) was found to be inadequate in both Test 2 and Test 3. Among parts programmed by the better (P2) method, consistent increases in functional failures were observed only for TI parts in the 200°C test (see Table 15). The activation energy (E_o) for loss of charge in single transistors of the type used in 2708 UV-PROMs was reported[2] to be 0.8 eV. Using this value and assuming the dependence of time before failure (t) upon temperature (T) to be the Arrhenius equation, $t = t_o \exp(-E_o/kT)$, then the time duration at 125°C, the military temperature limit, after which failures similar to those observed in test 3E would be expected is longer by a factor of $\exp E_o(1/kT_2 - 1/kT_1) = 40.4$. Therefore the time at 125°C equivalent to 768 h at 200°C, when the failures seemed to begin in test 3E, is 3.10×10^4 hours, or more than 3.5 years. This certainly is longer than any anticipated storage at 125°C for UV-PROMs in actual military systems applications. Therefore it appears that data retention during storage is adequate for these devices.

Write-Erase Endurance Test

Five devices from each of Intel and TI were repeatedly programmed and erased in order to study the effects of an excessive number of write-erase cycles. A Data I/O Corporation Programmer V PROM programmer[4] was used for the programming. It checks for verification after every programming loop and then performs 80 additional loops when the UV-PROM verifies.* (For the last few cycles of the test, some Intel parts were programmed on the S-3260, using Method P1 with 0.5 ms. pulses.) The erase cycle consisted of a minimum of one 20 minute exposure to UV followed by verification on the Data I/O to check that the device had erased. A failure to verify was followed by an additional exposure of five minutes and another verification, until erasing was complete. Full electrical testing at 25°C was accomplished on the Tektronix S-3260 prior to this test and after each 5 program-erase cycles. All devices had similar program-erase histories before this test, as shown in Table 6, except SN302 which had been used during the characterization phase of this study.

TABLE 6. PROGRAM-ERASE TEST HISTORY

		Number of Program-Erase Cycles	
SN	Vendor	Prior to Test **	At End of Test
302	Intel	18	68
303	Intel	4	54
304	Intel	3	53
307	Intel	5	55
308	Intel	4	54
16	TI	4	54
17	TI	4	54
18	TI	4	54
19	TI	4	54
20	TI	4	54

*The Data I/O Programmer uses a 1 ms. pulsewidth.

**The number of program-erase cycles performed by the vendors before shipping was unknown.

Each part was programmed and erased 50 times during this test with no apparent electrical degradation. However, anomalies in programming and erase time requirements were observed. For the first five cycles, all ten parts programmed in 5 minutes or less, as is typical for these devices, and erased in 20 minutes. For cycles 6-15, three Intel parts (SN 302, 304 and 308) required approximately 9 minutes to program with no change in the TI parts. For cycles 16-20, all parts programmed in 4 to 5 minutes but the same three Intel devices required 5 to 10 minutes extra erase time. For cycles 21-50, the Intel parts required approximately 9 minutes to program and an additional 5 to 15 minutes to erase (a total erase time of 25 to 35 minutes). One TI part (SN 16) failed to erase in 20 minutes two times, once at the tenth cycle and the second time at the twelfth cycle. From that point on, all TI devices programmed in 4 to 5 minutes and erased within 20 minutes.

The Intel devices used in this test began to require extended programming and erasing times after a total of 8 program-erase cycles. The extended erasing times may simply be the result of the extra programming that was required and not due to any device fault. The programming characterization described in Section 3.3 also indicated that Intel parts require more programming loops than do TI parts. As long as each part is read out after it is reprogrammed to verify that the correct information has been stored, the changes in programming and erase times will not impair the ability of the UV-PROMs to retain data, since no degradation of electrical performance was noted. An erase duration of at least 30 minutes is recommended to avoid the nuisance of having to repeat the erase-verify cycle.

Influence of Ambient Light

Since UV-PROMs are erasable by ultraviolet light, they must not be exposed to light that could erase them accidentally. (A precaution that some users have taken is to cover the quartz window with an opaque label while the device is in use.) Since the ultraviolet content of incandescent lamps is small, they do not pose much of a threat to UV-PROMs. However, fluorescent lamps do emit some UV radiation. The influence of a fluorescent desk lamp, placed 1 foot away from

UV-PROMs, on their retention of data was investigated in test 3F of the Optimum Procedures Tests, described in Section 5.3. No significant changes in functional, DC or AC measurements were observed in the test specimens after 1000 h of exposure. Therefore normal room lighting does not appear to be a threat to the reliability of UV-PROMs. However, exposure to other radiations, such as sunlight and x-rays, should be avoided.

Calibration and Maintenance of UV Lamp

Radiation of wavelengths shorter than 388 nm is required to erase UV-erasable PROMs.[1] Such radiation can be conveniently provided by a low pressure mercury vapor lamp with a quartz envelope, which emits strongly at around 254 nm. A lamp of this type (Ultraviolet Products model S-52T) was used in this study. An elapsed time meter was attached to it upon receipt of the lamp in order to determine its actual operating history. Although the lamp manufacturer states that the tube life exceeds 10,000 hours, the useful light output will decrease with use. This can lead to an increase in the time required to erase UV-PROMs or to incomplete erasure, which may show up only at temperature extremes. Therefore periodic measurement of the lamp's output is desirable.

The output of the UV lamp was measured with a spectroradiometer (EG&G model 580 radiometer with model 585-11 monochromator). As expected, most of the UV radiation was emitted at 254 nm, with a bandwidth at half maximum of 11 nm. The output in this band was initially determined to be 11 mW/cm^2 at a distance of 1.75 inches from the bulb, which is approximately the position of the bottom of the tray used to support the UV-PROMs during erasing and as close as the spectroradiometer could be positioned. This figure is different than that given by the manufacturer, 14 mW/cm^2 at a distance of 1 inch, but the difference probably is the result of the greater distance from the bulb. A second measurement of the lamp intensity, made after it had operated for 28.4 hours, gave an intensity of 5.8 to 6.7 mW/cm^2, depending upon the position of the spectroradiometer. At the same time, the output was also measured with a digital radiometer (Ultraviolet Products model J260) having a 254 nm filter. This instrument was more convenient to use and easier to move around.

It gave readings as high as 14 mW/cm^2 at 1 inch from the bulb and a considerable variation in intensity with lateral position was noted. Therefore the lower second measurement obtained with EG&G radiometer is probably not due to aging of the lamp but rather due to a different position of the radiometer.

The operation of the filtered digital radiometer was found to be rapid and convenient. Therefore that type of instrument is recommended for measuring the output of the UV lamps used to erase UV-PROMs. A fixture should be made to attach the radiometer to the lamp in a reproducible manner. Calibration should be done after every 25 hours of lamp operation initially. Experience may eventually show that less frequent calibration is acceptable.

4.2 INPUT PROTECTION NETWORKS

The high impedance inputs of MOS devices are usually protected with diodes to prevent the gate oxide of the input transistors from being shorted out by electrostatic discharges during handling and assembly. The effectiveness of the input protection networks influences the manufacturing yield and if they are inadequate, the cost of the electronic system may be increased. In order to evaluate the input protections on the 2708 UV-PROMs, four Intel (SN 309, 313, 323, 331) and three TI (SN 103, 105, 107) devices were subjected to simulated electrostatic discharges of increasing amplitudes.

Pin pairs selected for stress application represented all combinations of input, output, chip select, program, V_{CC}, V_{BB}, V_{SS}, and V_{DD}, taken two at a time. Voltage stresses of both polarities were used to see if the damage thresholds were dependent on polarity but no such dependence was detected. All unstressed pins were unterminated during pin pair stress application. Prestress electrical performance parameter measurements and simple dc pin pair measurements before and after each stress application period were used to determine failure. A minimum of thirty pulses at ten second intervals were applied at each stress level to each pin pair under evaluation. The test circuit of Figure 7 was used to apply the stress.

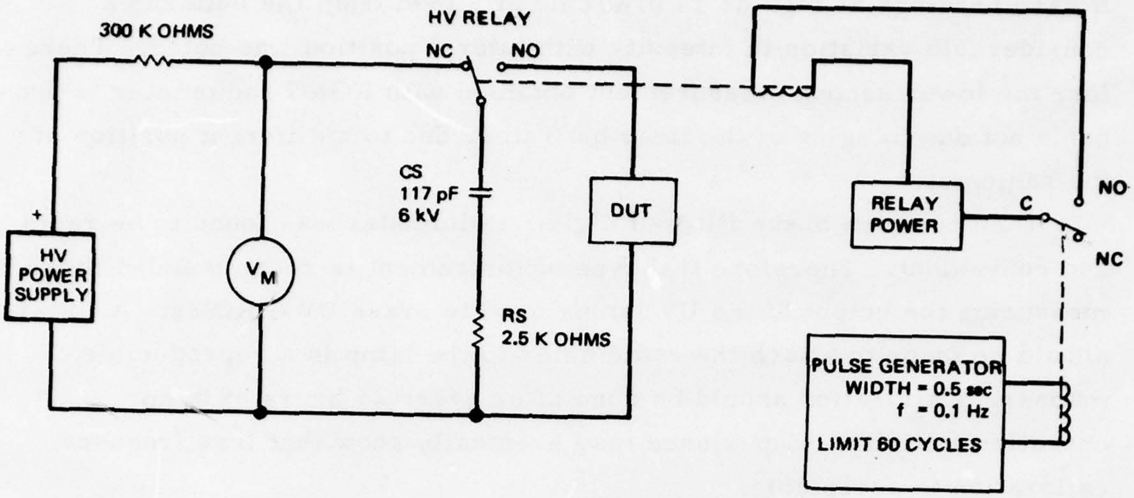


Figure 7. Electrostatic discharge stress circuit.

The results of tests on the four Intel devices are listed in Table 7. No failures were observed at 250V or less nor were any observed for pin pairs not listed. The threshold for damage was found to be between 250V and 500V and all four devices had failures at 750V or less. Most of the failures were associated with input pins and no ground pins were found to be sensitive with respect to any other pin.

The three TI devices consistently survived the 250 and 500 volt stress applications. They failed at a stress application of 1000 volt on the output pins with respect to the V_{SS} pin.

The damage threshold of the Intel UV-PROMs is considerably lower than the damage threshold of the TI parts. The observed values are all within the range measured for other MOS devices. Although the threshold for the Intel parts is at the low end of that range, damage thresholds at that level are not uncommon.

Another, more subjective, indication of sensitivity to static discharge damage is the failure history resulting from "normal handling". During the course of this study, over 200 UV-PROMs were subjected to an extensive test program; each was handled many times. Only two catastrophic failures occurred (both to the program pin line) and both are believed to

TABLE 7. ELECTROSTATIC DISCHARGE TEST RESULTS FOR FOUR INTEL MC2708 UV-PROMs

	Number of Pin Pairs at Each Stress Level					
	500V		750V		1000V	
Pin Pair Description	Tested	Failed	Tested	Failed	Tested	Failed
Input to input (A-A)	12	0	6	2	2	2
Input to output (A-O)	5	2	2	1	0	0
Output to output (O-O)	4	1	2	2	0	0
Output to program	2	0	2	1	0	0
Input to program	2	1	0	0	0	0
Input to chip select	3	2	1	1	0	0
TOTAL	28	6	13	7	2	2
PERCENT FAILED	21%		54%		100%	

be machine-induced during test and not the result of handling or insertion in test sockets. These observations plus the results of the electrostatic discharge tests show that all the normal precautions advised for the handling of MOS devices should be taken for UV-PROMs, but extreme measures should not be necessary.

4.3 THERMAL PROPERTIES

The thermal resistance from junction to ambient (θ_{JA}) of the UV-PROMs was determined using an adaptation of MIL-STD-883, Method 1012. Variations of the electrical characteristics of the input protection networks with temperature were used to determine the actual chip temperatures under various conditions.[6] (Although the input protection networks on the TI parts involve an FET connected as a diode, with its gate shorted to its source, the characteristics of this diode are similar to a standard diffused pn junction diode.)

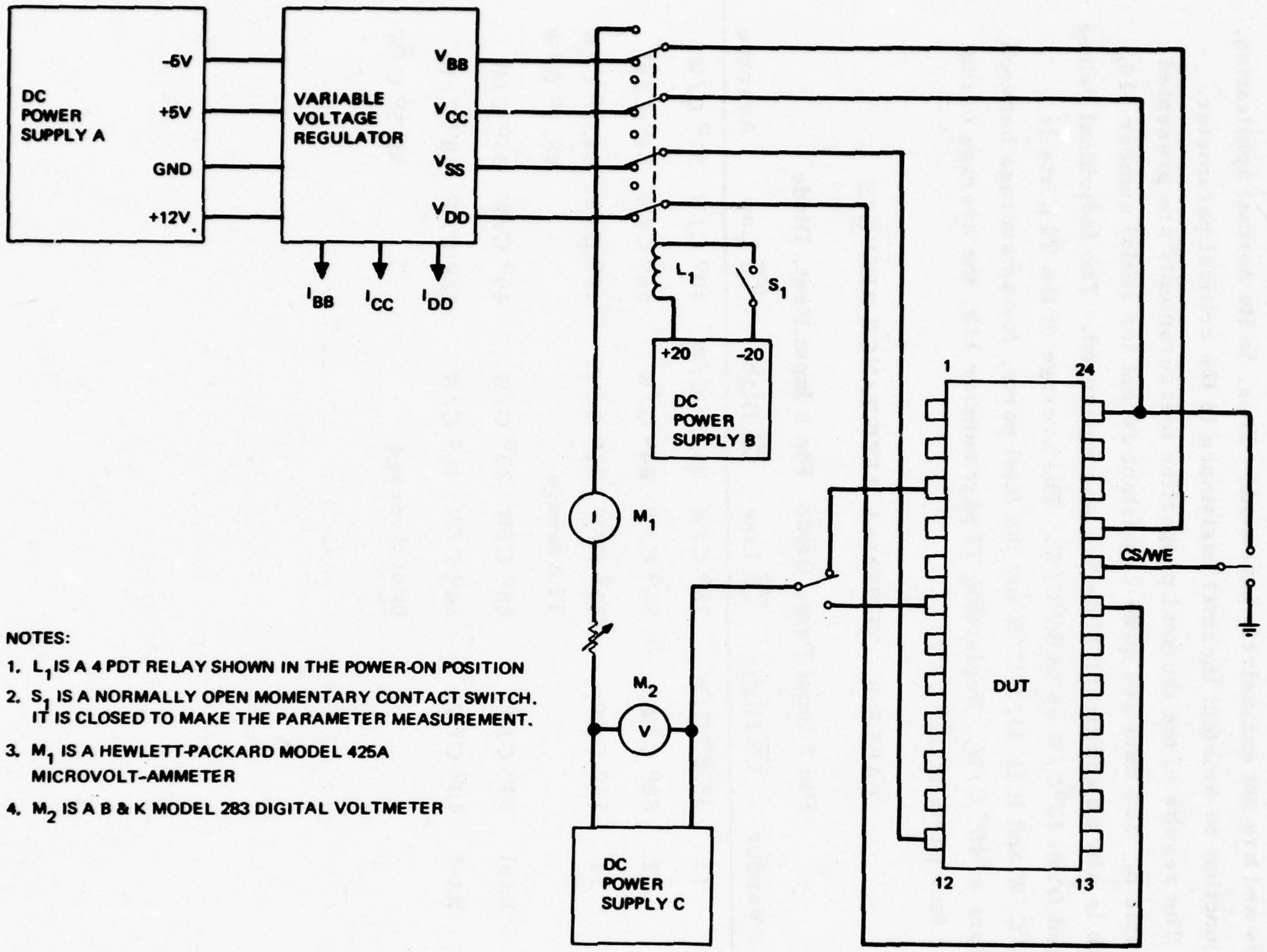
First, the forward voltage drop, V_F, and the reverse leakage current, I_R, were measured as a function of temperature, without power applied to the device. Next the parts were biased in the normal manner, as shown in Figure 8, and the power supplied to the device was measured. As the inputs and outputs were left open, the output power was considered to be insignificant. Temperature measurement was accomplished by removing the power with relay L_1, shown in Figure 8, while simultaneously connecting the test circuit to the input protection diode. Its characteristics were measured as rapidly as possible under the same test conditions as used for the temperature characterization. Only one reading was made before repowering the device to minimize cooling errors. Using these readings, the junction temperature was determined from the temperature characteristic plots. In the course of the test, it was found necessary to bias the parts to the maximum data sheet voltage ratings to get a sufficient junction temperature increase for accurate readings. Although both I_R and V_F were measured, only V_F was used in the temperature calculation because it was more stable and less subject to measurement error.

The thermal resistance was calculated by using the formula:

$$\theta_{JA} = \frac{T_J - T_A}{P_{IN} - P_{OUT}} ,$$

where

θ_{JA}	is the thermal resistance from junction to ambient
T_J	if the operating junction temperature (determined from the V_F temperature characteristic plot)
T_A	is the laboratory ambient temperature
P_{IN}	is the input power to the device
P_{OUT}	is the output power from the device


DC POWER SUPPLY A
-5V
+5V
GND
+12V
VARIABLE VOLTAGE REGULATOR
V_{BB}
V_{CC}
V_{SS}
V_{DD}
I_{BB}
I_{CC}
I_{DD}
L_1
S_1
+20
-20
DC POWER SUPPLY B
M_1
M_2
V
DC POWER SUPPLY C
1
24
DUT
12
13
CS/WE

NOTES:

1. L_1 IS A 4 PDT RELAY SHOWN IN THE POWER-ON POSITION
2. S_1 IS A NORMALLY OPEN MOMENTARY CONTACT SWITCH. IT IS CLOSED TO MAKE THE PARAMETER MEASUREMENT.
3. M_1 IS A HEWLETT-PACKARD MODEL 425A MICROVOLT-AMMETER
4. M_2 IS A B & K MODEL 283 DIGITAL VOLTMETER

Figure 8. Block diagram of UV-PROM thermal resistance measurement circuit.

Junction-to-ambient, rather than junction-to-case, thermal resistance was measured because the devices are normally mounted on printed circuit cards and are not extensively heat sunk. Thus, in its normal application, the junction-to-ambient thermal resistance is the critical parameter.

The results of the thermal properties measurements are presented in Table 8. The data are quite consistent except for serial number 110, which is why an additional TI device was measured. The individual values ranged from 12°C/W up to 86°C/W. The average of the TI parts is 48.5°C/W and it is 31.5°C/W for the Intel parts, for an average between vendors of 40° C/W. Neglecting TI part number 110, the average of the other four parts is 31° C/W.

TABLE 8. THERMAL RESISTANCE RESULTS

		Pin 3 Input Prot. Diode		Pin 6 Input Prot. Diode		
SN	Vendor	$\overline{CS}$ High	$\overline{CS}$ Low	$\overline{CS}$ High	$\overline{CS}$ Low	Average
10	TI	38.5° C/W	36° C/W	33.5° C/W	40° C/W	37° C/W
110	TI	80° C/W	86° C/W	84° C/W	86° C/W	84° C/W
96	TI	15° C/W	33° C/W	31° C/W	19° C/W	24.5° C/W
			TI Average			48.5° C/W
332	Intel	39° C/W	28° C/W	23° C/W	49° C/W	35° C/W
335	Intel	40° C/W	24° C/W	36° C/W	12° C/W	28° C/W
			Intel Average			31.5° C/W

Thermal resistance is a function of the package design and material, die bond material, die bond integrity, and the size of the die. Large variations (2:1 or 3:1) in the junction-to-case thermal resistance on parts from a single production run are not uncommon. With similar packages, die bond techniques, and die sizes, a greater variation is to be expected among the parts of a single supplier than among the average thermal resistances of several suppliers. In this study, the die sizes and the packages of both suppliers were very similar. The observed variations in thermal resistance are attributed to variations in the die attach process peculiar to each manufacturing line. There is no significant difference in the results for the two vendors.

According to Signetics' Bipolar and MOS Memory Data Manual (June 1977, p. 332), $\theta_{JA} = 65^{\circ}$ C/W for a 24 pin side-brazed lead ceramic package similar to that used for the military grade UV-PROMs studied in this program. Personnel at Signetics indicated that their value was very conservative; i.e., likely to be high. Therefore their value is consistent with the values obtained in this study.

Experience in these tests indicates that the power dissipations at 125°C ambient and nominal supply voltages are about 500 mW for the Intel 2708 UV-PROM and about 400 mW for the TI device. (The Intel M2708 data sheet states 750 mW maximum at 100°C and the TI TMS2708JL data sheet states 800 mW maximum at 70°C. The power dissipation decreases at higher temperatures because the supply currents decrease.) Taking the worst case power dissipations observed for each manufacturer's parts (see Table 8), at 125°C ambient the maximum junction temperatures will be approximately $125^{\circ}\text{C} + (49^{\circ}\ \text{C/W})(.5\ \text{W}) = 149.5^{\circ}\text{C}$ for the Intel device and $125^{\circ}\text{C} + (86^{\circ}\ \text{C/W})(.4\ \text{W}) = 159.4^{\circ}\text{C}$ for the TI device. These values are low enough to permit reliable operation of these UV-PROMs over the full military temperature range (-55°C to $+125^{\circ}$C).

5. OPTIMUM PROCEDURES TESTS

The objective of these tests was to establish the optimum procedures for programming, erasing, and burning-in of UV-PROMs. 8192-bit devices obtained from Intel and Texas Instruments were used in equal numbers in all tests. All parts were put through the screening tests described in Section 2 and so had been programmed and erased at least three times before the start of these tests. A few devices were programmed and erased more than 5 times. Individual records were maintained so the entire program-erase history of each part was known.

Tests already described in Section 2.2 showed that optimum programming requires additional programming loops beyond those necessary to obtain a verified readout at nominal voltages and 25°C. Two methods, designated P1 and P2, were evaluated in the operating life test and the data retention under storage test:

P1: 0.5 msec programming pulse width, 80 additional programming loops after initial verification at nominal voltages.

P2: 0.5 msec programming pulse width, 200 loops. (This is consistent with the method recommended on the manufacturers' data sheets.)

Although P2 is the "standard" method, P1 would have two advantages, if it is shown to be feasible: (1) Less time is required, since most devices verify after less than 10 programming loops. (2) Determining the actual number of programming loops required is a possible means of detecting unusual parts that probably should not be used for high reliability applications.

All programming and readout measurements for these tests were done on the Tektronix S-3260 automated test system in order to obtain nearly uniform conditions for both the methods. The programming pulse magnitude was 26V ± 1V. Bias was maintained during cool-down on all parts that were powered at high temperature.

The Optimum Procedures Tests are listed in Table 9. In the following subsections, each of the three groups of tests is described and the pertinent results are presented and discussed.

TABLE 9. OPTIMUM PROCEDURES TEST

Test Code	Test Description	Test Temperature
1	Erase Characteristics	Ambient
2A	Operating Life Test	100°C
2B	Operating Life Test	125°C
3A	Data Retention During Biased Storage	125°C
3B	Data Retention During Unpowered Storage	Ambient
3C	Data Retention During Unpowered Storage	125°C
3D	Data Retention During Unpowered Storage	150°C
3E	Data Retention During Unpowered Storage	200°C
3F	Data Retention During Exposure to Fluorescent Light	Ambient

Note: Test duration is 1000 h for all tests except Test 1.

5.1 TEST 1. ERASE CHARACTERISTICS

Objective: To determine the ultraviolet light exposure duration necessary to completely erase the UV-PROMs.

Stored data: Checkerboard data pattern.

Readout temperatures (°C): -55, 25, 100, 125.

Readout voltages at each temperature: Nominal, nominal ±5 percent, nominal ±10 percent (five values).

Quantity of parts used: 20 Intel, 20 TI. (These parts were reused for other tests.)

Procedure: Program 10 Intel and 10 TI parts with method P1; program the rest with method P2. Verify all parts at all readout temperatures and voltages. Erase all parts for 4 minutes, then perform readouts at all temperatures and voltages. Repeat after additional erase durations until all parts are completely erased.

The results of the erase characteristics test are summarized in Table 10. As expected from the initial experience with the two vendors' parts (see Section 2.2), the Intel devices generally required a longer time to erase. However all devices used in this test were completely erased in 20 minutes, which is consistent with the nominal durations recommended by the vendors (30 m by Intel and 20-30 m by TI).

A significant difference between the two programming methods, particularly for the Intel devices, is that erasing was quicker for the devices programmed by method P2. Although the total number of programming loops was less for method P1, the devices programmed by this method required a significantly longer erasure. Method P1 involved reading out the device after each program loop until it finally verified, then 80 more loops were performed. Before each readout, power was removed from the device and the conditions for readout were established before power was reapplied. Method P2 did not require removing power until the end of 200 program loops. Near the beginning of this program, it was found that some devices did not retain data after power was removed for an extended period of time if they were programmed with only the minimum number of loops required to obtain verification.

TABLE 10. UV-PROM ERASE CHARACTERISTICS TEST RESULTS

Erase Duration (Minute)	Percent of Bits Erased Intel P1	Intel P2	TI P1	TI P2
4	0.01	45.34	39.05	75.28
6	0.04	63.94	92.11	98.73
10	77.40	96.89	100.00	100.00
15	98.68	100.00	100.00	100.00
20	100.00	100.00	100.00	100.00

5.2 TEST 2. OPERATING LIFE TEST

Objective: To obtain data on failure rate versus time in order to establish optimum burning-in of UV-PROMs.

Stored data: Binary count pattern.

Operating conditions: Dynamic readout, 1 MHz cycle rate (LSB), with TTL equivalent load on each output, nominal voltages (±5%).

Cumulative measurement times (hours): 0, 4, 24, 72, 168, 500, 768, 1000.

Measurement temperature (^oC): -55, 25, 100, 125.

Functional test voltages at each measurement temperature: Nominal, nominal ±5%, nominal ±10% (5 values).

Parts used and operating temperatures:

Test Code	Operating Temp.	Method P1		Method P2	
		Intel	TI	Intel	TI
2A	100^oC	371-380	51-60	381-390	81-90
2B	125^oC	351-360	91-100	361-370	50, 101, 103-110

Procedure: Program parts with methods P1 and P2 and verify all parts at all measurement temperatures and voltages. Place parts in operating life test fixtures at 100^oC and 125^oC (see table). Read out all parts and measure DC parameters at nominal voltages after cumulative measurement times listed above. In addition, all AC and DC parameters were measured at all four measurement temperatures after 768 h and after 1000 h.

The results of tests 2A and 2B are summarized in Table 11, which lists the number of UV-PROM devices which did not meet one or more specifications at one or more temperature-voltage conditions. There were ten

TABLE 11. NUMBER OF UV-PROMs FAILING FUNCTIONAL TESTS OR NOT MEETING DC SPECIFICATIONS DURING OPERATING LIFE TESTS

	Test 2A (100°C)				Test 2B (125°C)			
	Method P1		Method P2		Method P1		Method P2	
Time (Hours)	Intel	TI	Intel	TI	Intel	TI	Intel	TI
0	0 (3)*	0 (0)	0 (6)	0 (1)	0 (0)	0 (1)	0 (0)	0 (2)
4	0	6	0	1	0	0	0	0
24	0	0	0	0	0	0	0	0
72	1	0	0	3	0	1	0	0
168	0	1	0	0	1	1	0	0
500	0	0	0	0	1	1	0	0
768	0 (3)*	0 (1)	0 (3)	0 (3)	1 (2)	0 (1)	0 (4)	0 (2)
1000	0 (10)*	0 (10)	0 (10)	0 (9)	1 (10)	0 (10)	0 (10)	0 (10)

*In parentheses is given the total number of parts failing to meet specifications, AC and DC, plus those failing functional tests. The additional failures after 768 h and 1000 h were in t_{DF} and are attributed to an S-3260 fault because failures were not observed when parts were checked manually. Three parts also had some V_{OH} failures.

devices from each vendor in each programming method for each of the two tests and devices which did not meet specifications were retained throughout the tests. For the 100°C parts (test 2A), there were no functional test failures and no consistent change in DC parameters throughout the test. At the end of the test, most parts showed t_{DF} (output disable time) to be out of specification but these failures were not confirmed when some parts were later checked by visual monitoring of device waveforms while still connected to the S-3260. Therefore most of the t_{DF} failures are attributed to malfunction of the S-3260 tester.

For the 125°C parts (test 2B), one Intel part (SN 352) failed functional tests at 168 h and all following times and one TI part (SN 96) failed one functional test (at minimum supply voltages, -55°C) at 72h, 168 h and 500 h but passed subsequent functional tests. No other functional failures occurred. At 768 h, some AC parameters on nine parts were not within specification. At 1000 h, all parts did not meet specifications for t_{DF}. These failures could not be verified and therefore they are attributed to a malfunction in the S-3260, just as in test 2A. They are not considered to indicate any real limitation on the operating life of 2708 UV-PROMs. Distribution plots of AC parameters and one DC parameter at the beginning of this test and at its end are given in Appendix F.

In both 2A and 2B, there were no substantial changes in supply and leakage currents over the course of testing. Some of the random failures which occurred at various measurement points throughout the test did not repeat. This could be due to measurement errors such as poor pin connections during a particular measurement or to borderline conditions that did not consistently produce a failure. There was no significant difference in the number of failures between vendors or between programming methods.

Although changes are evident at the end of 1000 hours, substantially shorter time periods do not have significant effect on device operation. It is concluded that for burn-in purposes, 168 hours at 125°C is acceptable for these parts.

5.3 TEST 3. DATA RETENTION DURING STORAGE

Objective: To determine the long term decay rate of data stored in UV-PROMs.

Stored data: Diagonals unprogrammed, all other locations programmed.

Cumulative measurement times (hours): 0, 6, 40, 168, 500, 768, 1000.

Measurement temperatures (°C): -55, 25, 100, 125.

Functional test voltages at each measurement temperature: Nominal, nominal ±5%, nominal ±10% (5 values).

Quantity of parts used and storage conditions: Shown in Table 12.

Procedure: Program parts with methods P1 and P2 and verify all parts at all measurement temperatures and voltages. Place parts in storage conditions according to table above. Read out all parts and measure DC parameters at nominal voltages after cumulative measurement times listed above. In addition, all AC and DC parameters will be measured at all four measurement temperatures after approximately 768 h and after 1000 h.

Data retention during storage (Test 3) consists of three main parts: biased storage at 125°C, unpowered storage at four temperatures (25, 125, 150, and 200°C), and exposure to fluorescent light at room temperature. The retention of data is determined by the functional test. In addition DC parameters were measured at all measurement times and AC parameters were measured at the beginning, near the end, and at the end of the tests. The parts were programmed only once; no reprogramming was done.

The results for test 3A, biased storage at 125°C, are summarized in Table 13. The results of the measurements at the start of this test are given in Appendix B as an example of the data obtained. There were 20 functional tests performed at each measurement time: four temperature conditions and five voltage conditions at each temperature. Since five parts from each vendor were used for each of the two programming methods, the maximum possible number of test failures was 20 x 5 = 100 for each entry in Table 13. No functional failures were observed for programming

TABLE 12. DATA RETENTION DURING STORAGE, OPTIMUM PROCEDURES TEST 3

Test Code	Storage Conditions	Program Method P1		Program Method P2	
		Intel	TI	Intel	TI
3A	Biased (nominal voltages), equiv. TTL loads, fixed address, 125°C	341-345	21-25	346-350	26-30
	Unpowered:				
3B	Room temperature	300, 302, 303	15, 16, 17	304, 307, 308	18*, 19, 20
3C	125°C	310-312, 315, 316	31, 32, 34-36	318, 319, 321, 322, 324	37, 38, 40-42
3D	150°C	325-329	43, 45-48	336-340	61, 63, 64, 66, 67
3E	200°C	391-394, 400	68, 69, 75-77	401, 403-406	79, 80, 111-113
3F	Exposed to fluorescent light, room temperature	330, 333, 334	39*, 44*, 49*	407, 408, 409	65*, 78*, 114

*Failed one or more AC or DC screening test but passed all initial tests here.

TABLE 13. NUMBER OF FUNCTIONAL TEST FAILURES DURING TEST 3A (125°C, BIASED)

	Method P1		Method P2	
Time (Hours)	Intel	TI	Intel	TI
0	43	8	0	0
6	46	8	0	0
40	46	12	0	0
168	38	10	0	0
500	40	10	0	0
768	38	11	0	0
1000	37	19	0	0

Note: The maximum possible number of failures for each entry is 100 (see text). For Method P1, all five Intel parts had failures at all times and two TI parts had failures.

method P2. For method P1, there was a slight decrease in failures of the Intel parts with time, although all five parts had some failures at all measurement times. This decrease is attributed to borderline programming conditions at the start of the test. An increase with time was observed in the smaller number of TI failures, which involved two parts, in method P1. Most of the functional failures in this test were at the nominal ±10 percent power supply voltages. No significant changes in DC parameters occurred. However, AC timing parameter increases occurred toward the end of this test for both vendors, with changes first evident for programming Method P1. T_{DF} is the AC parameter which shows the most change, with all devices finally failing to meet the vendors' specifications at all temperatures for low voltages. (Many of these failures are believed due to a measurement problem, as discussed on page 51.)

Tests 3B through 3E are unbiased storage at room temperature and at three elevated temperatures. Test 3B at 25°C is primarily a control sample. For both 3B and 3C (125°C), there is no significant change during the tests for functional, DC and AC parameters. The results of the functional tests are given in Table 14. For test 3B, three parts from each vendor were used for each programming method so the maximum possible number of failures is 3 x 20 = 60. The failures observed for Intel P1 parts were distributed among all three samples, while only one TI part (SN 17) had failures. For test 3C, five parts were used in each group so the maximum possible number of failures was 100. The Intel failures were distributed among all five P1 samples and again only one TI part (SN 34) had failures. As usual, the functional failures were mostly at the wider (±10 percent) power supply limits and no failures were detected in parts programmed by method P2. Of the AC parameters, most failures were of access time (t_{ACC}) and output disable time (t_{DF}).*

The functional test results for tests 3D and 3E are summarized in Table 15. Five samples were used for each of these groups so the maximum possible number of failures is 100. Again no functional failures in parts programmed by method P2 were observed at 150°C. There is no significant change in the number of Intel P1 failures at either 150°C (where all five parts had functional failures at all measurement times) or at 200°C (where all five parts had failures but only four failed at any one time).

The most significant changes in data retention occurred for the TI parts at 200°C. A slight increase in functional failures (from one part to two parts) was observed at 150°C for those TI parts programmed by method P1, but even one TI part programmed by method P2 showed failures by the end of test 3E. The AC timing parameters, especially output disable time, had increased at the 768 hour measurements for both of these tests and 39 of the 40 parts failed one or more AC tests after 1000 h.* Input leakage currents increased but remained within vendors' specification limits.

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*See discussion of t_{DF} measurement problems on page 51.

TABLE 14. NUMBER OF FUNCTIONAL TEST FAILURES DURING STORAGE AT ROOM TEMPERATURE AND 125°C

	Test 3B (Room Temp.)				Test 3C (125°C)			
	Method P1		Method P2		Method P1		Method P2	
Time (Hours)	Intel	TI	Intel	TI	Intel	TI	Intel	TI
0	26	6	0	0	48	2	0	0
6	25	8	0	0	49	2	0	0
40	25	7	0	0	49	2	0	0
168	25	7	0	0	44	2	0	0
500	25	8	0	0	50	2	0	0
768	omitted		omitted		47	2	0	0
1000	24	8	0	0	49	2	0	0

Note: The maximum possible number of failures for each entry for test 3B is 60 and for test 3C it is 100 (see text). Of the parts programmed by Method P1, all Intel parts (three in test 3B and five in test 3C) had failures and one of the TI parts in each test had failures.

TABLE 15. NUMBER OF FUNCTIONAL TEST FAILURES DURING STORAGE AT 150°C AND 200°C

Time (Hours)	Test 3D (150°C)				Test 3E (200°C)			
	Method P1		Method P2		Method P1		Method P2	
	Intel	TI	Intel	TI	Intel	TI	Intel	TI
0	45	1	0	0	28	3	0	0
6	44	1	0	0	34	3	0	0
40	45	1	0	0	36	3	1	0
168	42	1	0	0	27	3	0	0
500	48	3	0	0	35	3	2	0
768	45	2	0	0	27	43	2	7
1000	38	2	0	0	30	44	0	20

Note: The maximum possible number of failures for each entry is 100 (see text). In both tests, all five Intel parts programmed by Method P1 failed one or more functional tests. In test 3D, Method P1, the number of TI parts with failures increased from one (through 168 h) to two (at 500 h and subsequently). In test 3E, Method P1, four TI parts failed. For the Method P2 parts in test 3E, two Intel parts and one TI part had functional failures.

Reliability studies of the 2708 UV-PROM conducted at Intel[2] included operating and storage life tests at temperatures higher than those employed in this study. Also, larger numbers of samples were used and the test methods were different. Therefore the results of the two studies cannot be directly compared. However, the results of this study are reasonably consistent with the Intel results.

The results of test 3F, where UV-PROMs were exposed to fluorescent light, are summarized in Table 16. The lamp used was a desk lamp containing two F15 T8-WW (17 inches long) bulbs and it was placed approximately one foot (30 cm) above the UV-PROMs. There were three devices in each of the four groups listed in Table 16 so the maximum possible number of functional failures was 60. As with the tests already discussed, programming method P2 appears to be more successful than P1. The functional failures observed for the Intel P1 devices were distributed among all three parts. No significant changes in functional, DC or AC measurements were observed in this test, indicating that fluorescent light is not a hazard to UV-PROMs. This is discussed more fully in Section 4.1.

TABLE 16. NUMBER OF FUNCTIONAL TEST FAILURES DURING EXPOSURE TO FLUORESCENT LIGHT (TEST 3F)

	Method P1		Method P2	
Time (Hours)	Intel	TI	Intel	TI
0	23	0	0	0
6	23	0	0	0
40	23	0	0	0
168	19	0	0	0
500	25	0	0	0
768	24	0	0	0
1000	21	0	0	0

Note: The maximum possible number of failures for each entry is 60 (see text). All of the three Intel parts programmed by Method P1 had functional failures.

For both Tests 2 and 3, parts programmed by method P1 are much more likely to fail to meet specifications than those programmed by method P2. This includes measurement voltage and temperature variations as well as the time and temperature stresses of the various tests.

Of the AC timing parameters, t_{DF} (output disable time) is apparently the most sensitive to test stress. However, as discussed in Section 3 and verified by one vendor, its value is very sensitive to test conditions and the output load circuit to be used for that measurement is not adequately defined. The apparent failures to meet the vendors' specifications for this parameter at the end of tests 3A, 3D and 3E probably resulted from a slight change in the operation of the S-3260 tester in the automatic mode that was not revealed by the self-test program for the S-3260 (VERDICT), which was run twice each day. This is suspected because visual monitoring of waveforms of twelve parts from those tests did not verify the failures. Perhaps the use of an active load, instead of the passive one shown in Figure 5, might have improved the results, although it would be difficult to obtain one that would simulate the desired worst case specifications and it could be inconvenient to use. The other AC parameters that were sensitive to the test stresses were access time and chip select to output delay time.

Storage for extended periods of time at elevated temperatures is undesirable. After 1000 hours, some changes were seen at 150°C and substantial changes occurred at the 200°C storage temperature. It is not known what fraction of these changes was due to normal microcircuit wearout mechanisms, such as electromigration and formation of intermetallic compounds, and what fraction was due to mechanisms unique to UV-PROMs, such as loss of charge from the floating gate.

6. FAILURE ANALYSIS

One TI sample (SN 11, one of the set-up samples) failed during a programming attempt. The reported failure mode was sinking excessive (up to 200 mA) current at the program pin (pin 18). That input became essentially a short circuit, accepting whatever current was supplied to it. A visual inspection made prior to removal of the window from the package showed no obvious evidence of overstress anywhere along the program input stripe, which runs completely around the perimeter of the chip. After the window was removed to enable inspection of the chip under high (1000 X) magnification, a sub-oxide arc-over, typical of voltage overstress, was observed along the program line metallization strip near a contact window.

One of the Intersil samples, SN 500, failed as a result of probable overstress on the programming line during programming characterization with a 28V pulse amplitude. This part was also found to have a minute sub-oxide arc-over along the programming line metallization stripe. This suggests that the TI failure may also have been caused by accidental overstress during programming.

No catastrophic failures were detected during the 1000 hour life tests and no other failure analyses were performed. Since the number of failures was so small, no specific recommendations to effectively remove a specific type of failure were incorporated in the draft specification prepared under this contract.

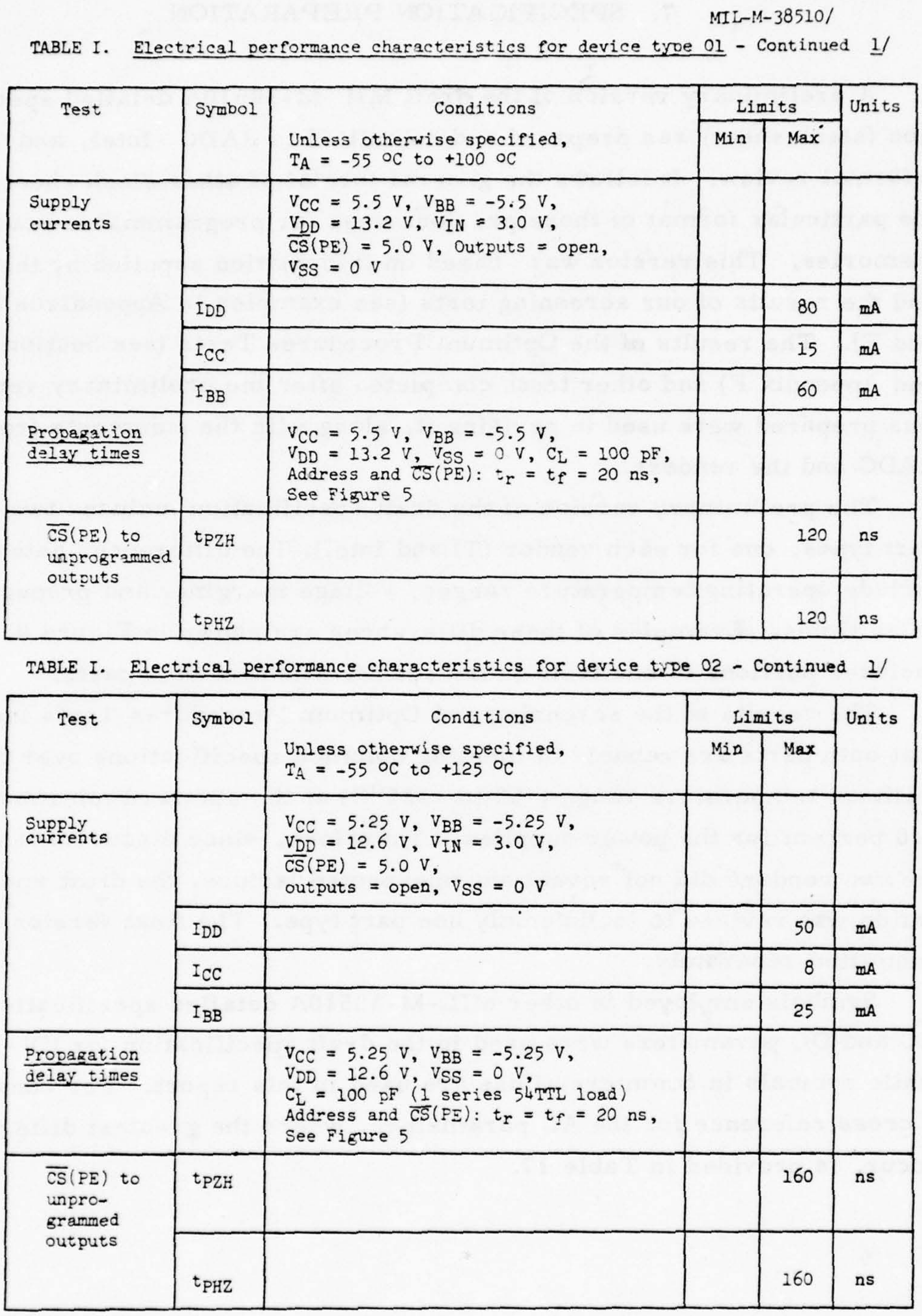
7. SPECIFICATION PREPARATION

A preliminary version of the draft MIL-M-38510A detailed specification (slash sheet) was prepared and submitted to RADC, Intel, and TI for informal review. It follows the general format of other slash sheets and the particular format of those previous ones for programmable read-only memories. This version was based on information supplied by the vendors and the results of our screening tests (see examples in Appendices D and E). The results of the Optimum Procedures Tests (see Section 5 and Appendix F) and other tests completed after the preliminary version was prepared were used in revising it, along with the comments from RADC and the vendors.

The preliminary version of the draft specification included two different part types, one for each vendor (TI and Intel). The differences between parts include operating temperature ranges, voltage margins, and propagation delay times. Examples of these differences are shown in Figure 9, which includes portions of one table in the specification for both parts.

The results of the screening and Optimum Procedures Tests indicated that both parts are capable of meeting common specifications over the full military temperature range (-55 to +125°C) at the standard tolerance of ±10 percent for the power supplies. Therefore, since discussions with the two vendors did not reveal any unexpected factors, the draft specification was revised to include only one part type. The final version was submitted separately.

Symbols employed in other MIL-M-38510A detailed specifications for AC and DC parameters were used in the draft specification for UV-PROMs, while symbols in commercial use are used in this report. For convenience, a cross reference for the AC parameters, where the greatest differences occur, is provided in Table 17.



MIL-M-38510/

TABLE I. Electrical performance characteristics for device type 01 - Continued 1/

Test	Symbol	Conditions Unless otherwise specified, $T_A = -55\ ^{o}C$ to $+100\ ^{o}C$	Limits Min	Limits Max	Units
Supply currents		$V_{CC} = 5.5$ V, $V_{BB} = -5.5$ V, $V_{DD} = 13.2$ V, $V_{IN} = 3.0$ V, $\overline{CS}$(PE) = 5.0 V, Outputs = open, $V_{SS} = 0$ V			
	I_{DD}			80	mA
	I_{CC}			15	mA
	I_{BB}			60	mA
Propagation delay times		$V_{CC} = 5.5$ V, $V_{BB} = -5.5$ V, $V_{DD} = 13.2$ V, $V_{SS} = 0$ V, $C_L = 100$ pF, Address and $\overline{CS}$(PE): $t_r = t_f = 20$ ns, See Figure 5			
$\overline{CS}$(PE) to unprogrammed outputs	t_{PZH}			120	ns
	t_{PHZ}			120	ns

TABLE I. Electrical performance characteristics for device type 02 - Continued 1/

Test	Symbol	Conditions Unless otherwise specified, $T_A = -55\ ^{o}C$ to $+125\ ^{o}C$	Limits Min	Limits Max	Units
Supply currents		$V_{CC} = 5.25$ V, $V_{BB} = -5.25$ V, $V_{DD} = 12.6$ V, $V_{IN} = 3.0$ V, $\overline{CS}$(PE) = 5.0 V, outputs = open, $V_{SS} = 0$ V			
	I_{DD}			50	mA
	I_{CC}			8	mA
	I_{BB}			25	mA
Propagation delay times		$V_{CC} = 5.25$ V, $V_{BB} = -5.25$ V, $V_{DD} = 12.6$ V, $V_{SS} = 0$ V, $C_L = 100$ pF (1 series 54TTL load) Address and $\overline{CS}$(PE): $t_r = t_f = 20$ ns, See Figure 5			
$\overline{CS}$(PE) to unprogrammed outputs	t_{PZH}			160	ns
	t_{PHZ}			160	ns

Figure 9. Portions of Table I from the preliminary copy of the draft MIL-M-38510A detailed specifications, illustrating the differences between UV-PROM type 01 (Intel) and type 02 (TI).

TABLE 17. CROSS REFERENCE FOR AC PARAMETERS SYMBOLS

This Report	Draft Specification
t_{ACC}	t_{PLH}, t_{PHL}
t_{CO}	t_{PZH}, t_{PZL}
t_{DF}	t_{PHZ}, t_{PLZ}
t_{OH}	t_{PVX}

8. CONCLUSIONS

A study of 8192-bit UV-PROMs has been performed. Initially, difficulties were experienced in screening tests due to insufficient programming and incorrect specifications. After these problems were corrected, 91 percent of the parts were found to meet the vendors' specifications over the temperature range -55°C to +125°C with power supply variations of ±10 percent. "Shmoo" plots obtained during electrical characterization tests confirmed that both Intel and TI parts can operate with the usual power supply voltage tolerance of ±10 percent with comfortable margins over the full military temperature range (-55°C to +125°C). The vendors' criterion for programming, namely that the product of the number of programming loops and the programming pulse width should be at least 100 ms, was found to be adequate. The programming pulse amplitude specification of (26 ±1) V is consistent with that criterion and safe.

The retention of data during storage was found to be adequate. No electrical degradation as a result of more than 50 write-erase cycles was detected, although increases in the number of programming cycles and erase duration required for Intel parts was observed. Therefore it is always necessary to read out UV-PROMs after programming them, as with any other type of PROM, and they should be exposed to the UV lamp for at least 30 minutes when erasing. This duration will also allow for some degradation of the UV lamp, which should be calibrated every 25 hours until its long term operating characteristics are determined, after which less frequent intervals would probably suffice.

The input protection networks of both the TI and Intel parts were found to afford adequate protection against electrostatic discharge. However, the usual precautions for handling MOS devices should be taken with UV-PROMs. Measurements of the thermal resistance and input power showed that the maximum junction temperature at 125°C ambient will be 160°C or less. This is low enough for reliable operation over the full military temperature range. Such operation was demonstrated by operating life tests at 100°C and at 125°C. These tests also indicated that the standard burn-in duration of 168 h at 125°C would be adequate for UV-PROMS.

One of the AC parameters, the output disable time (t_{DF}), was apparently outside of specifications on nearly all parts at the end of the operating life tests and at the end of the 150°C and 200°C storage tests. The widespread failure of this parameter for devices from both vendors is not understood but is believed due to a malfunction of the S-3260 tester, not an inherent weakness of the devices, since manual retest did not substantiate the failures. Other possible causes could be an error in the definition of t_{DF} or the use of an inadequate output load circuit. Nevertheless, storage or operation of these devices at temperatures in the neighborhood of 125°C should be limited to durations of less than one year.

Programming the UV-PROMs with only the minimum number of loops required to make them verify at room temperature and nominal supply voltages left them liable to fail to verify at temperature and voltage extremes. Although an additional 80 programming loops would enable them to verify at all conditions initially, this method was found to be inadequate in the 1000 hour life tests. The recommended procedure is that given by the vendors: the product of the number of programming loops and the programming pulse width (in milliseconds) should be at least 100 ms.

Only two catastrophic failures occurred during this study. Both were found to be caused by sub-oxide arc-overs along the programming metallization line. They are believed to result from the application of excessive voltage during programming. This is not a hazard as long as the programming pulse amplitude is restricted to its specified range (26V ±1V). Gross and fine leak tests during screening and again after Optimum Procedure Test 3 did not reveal any problem with sealing of the quartz window on the packages. (A new electrostatic discharge failure mode associated with quartz windows was recently discovered[5] and can be avoided by not subjecting UV-PROMs to freeze spray.)

A draft of a MIL-M-38510A detailed specification (slash sheet) for 8,192-bit UV-PROMs was prepared. Preliminary copies were sent to RADC, Intel, and TI for comments. Their responses were used to make revisions for the final draft which was submitted separately.

This study of ultraviolet-erasable PROMs showed that these devices can meet typical military specifications and those that do should perform reliably in military applications. Although many questions about UV-PROMs have been answered, there are two questions that warrant further investigation:

- Why do parts programmed by the method recommended by the vendors appear to erase easier but retain data better than those programmed by method P1 (see page 38)?
- Why did so many parts apparently fail to meet the output disable time specifications at the end of the elevated temperature storage and operating life tests?

There are other topics beyond the scope of this study that also could be investigated:

- Military grade 2708 UV-PROMs are apparently available now from additional vendors, e.g., Motorola, Fairchild, National, and Signetics. Parts from these vendors should be evaluated to see if they meet the draft specification.
- Larger UV-PROMs with twice the bit capacity (16,384 bits) and larger are now available and should be evaluated for military applications.
- New versions of UV-PROMs requiring only one 5V power supply (Intel's 2758 and TI's 2532, for example) and devices with low power requirements (e.g., TI's 27L08) offer some advantages. They should be evaluated to determine whether they can be included as additional part types in the detailed specification drafted in this study.

APPENDIX A

SUMMARY OF FUNCTIONAL, DC AND AC PARAMETERS SCREENING TESTS

Following are summaries of the results of the screening tests. The voltage limits for each summary are given at the top of each page. The number of UV-PROMs which failed to meet each vendor's specification (see Table 3) for the indicated parameters are given. Below that is a list of the serial numbers of the parts that failed at least one condition. (See Appendix D for example data plots.)

ALL PARTS @ NOMINAL ±10% V_{CC}, V_{BB}, V_{DD}

TOTAL POPULATION = 202

TEMPERATURE (°C)	25	-55	100	125
FUNCTIONAL	4	4	4	2
TACC	1	3	5	5
TCO	1	4	2	2
TDF	6	9	8	8
TOH	0	0	0	0
ILIH	0	0	1	0
ILIL	0	0	0	0
VOL	2	0	3	3
VOH1	1	0	2	3
VOH2	1	0	1	2
ILO	0	0	0	0
IDD	0	0	0	0
ICC	0	0	0	0
IBB	0	0	0	0

18
33
39
44
49
65
78
301
306
317
501
502
503
504
505

15 TOTAL FAILURES
7 TEXAS INSTRUMENTS FAILURES
5 INTERSIL FAILURES
3 INTEL FAILURES

INTEL @ NOMINAL ±10% V_{CC}, V_{BB}, V_{DD}

TOTAL SAMPLE = 103

TEMPERATURE (°C)	25	-55	100	125
FUNCTIONAL	0	0	0	0
TACC	0	0	2	2
TCO	0	0	0	1
TDF	1	2	2	2
TOH	0	0	0	0
ILIH	0	0	0	0
ILIL	0	0	0	0
VOL	1	0	2	2
VOH1	0	0	2	2
VOH2	0	0	1	1
ILO	0	0	0	0
IDD	0	0	0	0
ICC	0	0	0	0
IBB	0	0	0	0

301
306
317
3 TOTAL FAILURES

TEXAS INSTRUMENTS @ NOMINAL ±10% V_{CC}, V_{BB}, V_{DD}

TOTAL SAMPLE = 94

TEMPERATURE (°C)	25	-55	100	125
FUNCTIONAL	0	1	0	0
TACC	0	2	2	1
TCO	0	3	1	0
TDF	0	3	1	1
TOH	0	0	0	0
ILIH	0	0	1	0
ILIL	0	0	0	0
VOL	0	0	1	1
VOH1	0	0	0	1
VOH2	0	0	0	1
ILO	0	0	0	0
IDD	0	0	0	0
ICC	0	0	0	0
IBB	0	0	0	0

18
33
39
44
49
65
78

7 TOTAL FAILURES

TEXAS INSTRUMENTS @ NOMINAL ±5% V_{CC}, V_{BB}, V_{DD}

TOTAL SAMPLE = 94

TEMPERATURE (°C)	25	-55	100	125
FUNCTIONAL	0	0	0	0
TACC	0	0	2	1
TCO	0	0	1	0
TDF	0	1	1	1
TOH	0	0	0	0
ILIH	0	0	1	0
ILIL	0	0	0	0
VOL	0	0	1	1
VOH1	0	0	0	1
VOH2	0	0	0	1
ILO	0	0	0	0
IDD	0	0	0	0
ICC	0	0	0	0
IBB	0	0	0	0

18
33
39
44
49

5 TOTAL FAILURES

INTERSIL @ NOMINAL ±10% V_{CC}, V_{BB}, V_{DD}

TOTAL SAMPLE = 5

TEMPERATURE (°C)	25	-55	100	125
FUNCTIONAL	4	3	4	2
TACC	1	1	1	2
TCO	1	1	1	1
TDF	5	4	5	5
TOH	0	0	0	0
ILIH	0	0	0	0
ILIL	0	0	0	0
VOL	1	0	0	0
VOH1	1	0	0	0
VOH2	1	0	0	0
ILO	0	0	0	0
IDD	0	0	0	0
ICC	0	0	0	0
IBB	0	0	0	0

501
502
503
504
505

5 TOTAL FAILURES

APPENDIX B

EXAMPLE OF OPTIMUM PROCEDURES TEST RESULTS

Following is one of the summaries of electrical tests performed for the Optimum Procedures Tests. The AC parameter measurements and the functional tests were performed at five power supply voltages: 1 = nominal, 2 = nominal +5 percent, 3 = nominal -5 percent, 4 = nominal +10 percent, 5 = nominal -10 percent. The DC parameters were measured only at the nominal power supply voltages. At each condition for each parameter, the number of devices which failed to meet each vendor's specifications (see Table 3) is given. Devices programmed by the two methods tested, P1 and P2 (see Section 5) are listed separately. The serial numbers of the devices which failed one or more parameter are given near the bottom of each page. (See Appendix F for example data plots.)

```
              SUMMARY OF FAILURES,   TEST3(A)  END-POINT:  0

                                      TEXAS INSTRUMENT
PGM METHOD:      --------- P1 -------                 --------- P2 -------
TEMP ------>     25    -55    100    125              25    -55   100    125

TACC  1          0      0      0      1               0      0     0      0
TACC  2          0      0      1      1               0      0     0      0
TACC  3          0      0      1      2               0      0     0      0
TACC  4          0      0      2      2               0      0     0      0
TACC  5          1      0      2      2               0      0     0      0
TCO   1          0      0      0      1               0      0     0      0
TCO   2          0      0      0      0               0      0     0      0
TCO   3          0      0      1      1               0      0     0      0
TCO   4          0      0      1      1               0      0     0      0
TCO   5          1      0      2      2               0      0     0      0
TDF   1          0      0      0      0               0      0     0      0
TDF   2          0      0      0      1               0      0     0      0
TDF   3          0      0      1      1               0      0     0      0
TDF   4          0      0      1      2               0      0     0      0
TDF   5          1      0      2      2               0      0     0      0
TOH   1          0      0      0      0               0      0     0      0
TOH   2          0      0      0      0               0      0     0      0
TOH   3          0      0      0      0               0      0     0      0
TOH   4          0      0      0      0               0      0     0      0
TOH   5          0      0      0      0               0      0     0      0

                                          INTEL
PGM METHOD:      --------- P1 -------                 --------- P2 -------
TEMP ------>     25    -55    100    125              25    -55   100    125

TACC  1          0      0      0      1               0      0     0      0
TACC  2          0      0      1      2               0      0     0      0
TACC  3          0      0      3      4               0      0     0      0
TACC  4          3      1      5      5               0      0     0      0
TACC  5          5      4      5      5               0      0     0      0
TCO   1          0      0      0      0               0      0     0      0
TCO   2          0      0      0      0               0      0     0      0
TCO   3          0      0      0      1               0      0     0      0
TCO   4          0      0      2      4               0      0     0      0
TCO   5          4      2      5      5               0      0     0      0
TDF   1          0      0      0      0               0      0     0      0
TDF   2          0      0      0      1               0      0     0      0
TDF   3          1      0      4      4               0      0     0      0
TDF   4          4      3      5      5               0      0     0      0
TDF   5          5      5      5      5               0      0     0      0
TOH   1          0      0      0      0               0      0     0      0
TOH   2          0      0      0      0               0      0     0      0
TOH   3          0      0      0      0               0      0     0      0
TOH   4          0      0      0      0               0      0     0      0
TOH   5          0      0      0      0               0      0     0      0

FAILED THE FOLLOWING SERIAL NUMBERS:
  23 ,   24 ,   25 ,  341 ,  342 ,  343 ,  344 ,  345 ,

  8 TOTAL FAILURES        3 T.I.  FAILURES        5 INTEL FAILURES
```

```
              SUMMARY OF FAILURES,    TEST3(A)END-POINT:  0

                                       TEXAS INSTRUMENT
PGM METHOD:       --------- P1 -------             --------- P2 -------
TEMP ------>      25     -55    100    125           25     -55    100    125

FUNCTIONAL 1      0      0      0      0             0      0      0      0
FUNCTIONAL 2      0      0      0      0             0      0      0      0
FUNCTIONAL 3      0      0      0      1             0      0      0      0
FUNCTIONAL 4      0      0      1      1             0      0      0      0
FUNCTIONAL 5      1      0      2      2             0      0      0      0
ILIH              0      0      0      0             0      0      0      0
ILIL              0      0      0      0             0      0      0      0
VOL               0      0      0      0             0      0      0      0
VOH1              0      0      0      0             0      0      0      0
VOH2              0      0      0      0             0      0      0      0
ILO               0      0      0      0             0      0      0      0
IDD               0      0      0      0             0      0      0      0
ICC               0      0      0      0             0      0      0      0
IBB               0      0      0      0             0      0      0      0


                                             INTEL
PGM METHOD:       --------- P1 -------             --------- P2 -------
TEMP ------>      25     -55    100    125           25     -55    100    125

FUNCTIONAL 1      0      0      0      0             0      0      0      0
FUNCTIONAL 2      0      0      0      0             0      0      0      0
FUNCTIONAL 3      1      0      2      3             0      0      0      0
FUNCTIONAL 4      4      3      5      5             0      0      0      0
FUNCTIONAL 5      5      5      5      5             0      0      0      0
ILIH              0      0      0      0             0      0      0      0
ILIL              0      0      0      0             0      0      0      0
VOL               0      0      0      0             0      0      0      0
VOH1              0      0      0      0             0      1      0      0
VOH2              0      0      0      0             0      0      0      0
ILO               0      0      0      0             0      0      0      0
IDD               0      0      0      0             0      0      0      0
ICC               0      0      0      0             0      0      0      0
IBB               0      0      0      0             0      0      0      0

FAILED THE FOLLOWING SERIAL NUMBERS:
   23 ,    25 ,   341 ,   342 ,   343 ,   344 ,   345 ,   348 ,

   8 TOTAL FAILURES        2 T.I.  FAILURES        6 INTEL FAILURES
```

APPENDIX C

BIT MAPS FOR 2708 UV-PROMS

BIT MAP FOR INTEL 2708 UV-PROM

A0							1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	1
A1							0	0	1	1	0	0	0	0	0	0	1	1	1	1	1	1
A2							0	0	0	0	1	1	0	0	1	1	0	0	1	1	1	1
A3							0	0	0	0	0	0	1	1	1	1	1	1	0	0	1	1
	A9	A8	A7	A6	A5	A4	1	0	3	2	5	4	9	8	13	12	11	10	7	6	14	15
1	0	0	0	0	0	1																
0	0	0	0	0	0	0																
2	0	0	0	0	1	0																
3	0	0	0	0	1	1																
5	0	0	0	1	0	1																
4	0	0	0	1	0	0																
6	0	0	0	1	1	0																
7	0	0	0	1	1	1																
9	0	0	1	0	0	1																
8	0	0	1	0	0	0																
10	0	0	1	0	1	0																
11	0	0	1	0	1	1																
13	0	0	1	1	0	1																
12	0	0	1	1	0	0																
14	0	0	1	1	1	0																
15	0	0	1	1	1	1																
17	0	1	0	0	0	1																
16	0	1	0	0	0	0																
18	0	1	0	0	1	0																
19	0	1	0	0	1	1																
21	0	1	0	1	0	1																
20	0	1	0	1	0	0																
22	0	1	0	1	1	0																
23	0	1	0	1	1	1																
25	0	1	1	0	0	1																
24	0	1	1	0	0	0																
26	0	1	1	0	1	0																
27	0	1	1	0	1	1																
29	0	1	1	1	0	1																
28	0	1	1	1	0	0																
30	0	1	1	1	1	0																
31	0	1	1	1	1	1																
33	1	0	0	0	0	1																
32	1	0	0	0	0	0																
34	1	0	0	0	1	0																
35	1	0	0	0	1	1																
37	1	0	0	1	0	1																
36	1	0	0	1	0	0																
38	1	0	0	1	1	0																
39	1	0	0	1	1	1																
41	1	0	1	0	0	1																
40	1	0	1	0	0	0																
42	1	0	1	0	1	0																
43	1	0	1	0	1	1																
45	1	0	1	1	0	1																
44	1	0	1	1	0	0																
46	1	0	1	1	1	0																
47	1	0	1	1	1	1																
49	1	1	0	0	0	1																
48	1	1	0	0	0	0																
50	1	1	0	0	1	0																
51	1	1	0	0	1	1																
53	1	1	0	1	0	1																
52	1	1	0	1	0	0																
54	1	1	0	1	1	0																
55	1	1	0	1	1	1																
57	1	1	1	0	0	1																
56	1	1	1	0	0	0																
58	1	1	1	0	1	0																
59	1	1	1	0	1	1																
61	1	1	1	1	0	1																
60	1	1	1	1	0	0																
62	1	1	1	1	1	0																
63	1	1	1	1	1	1																

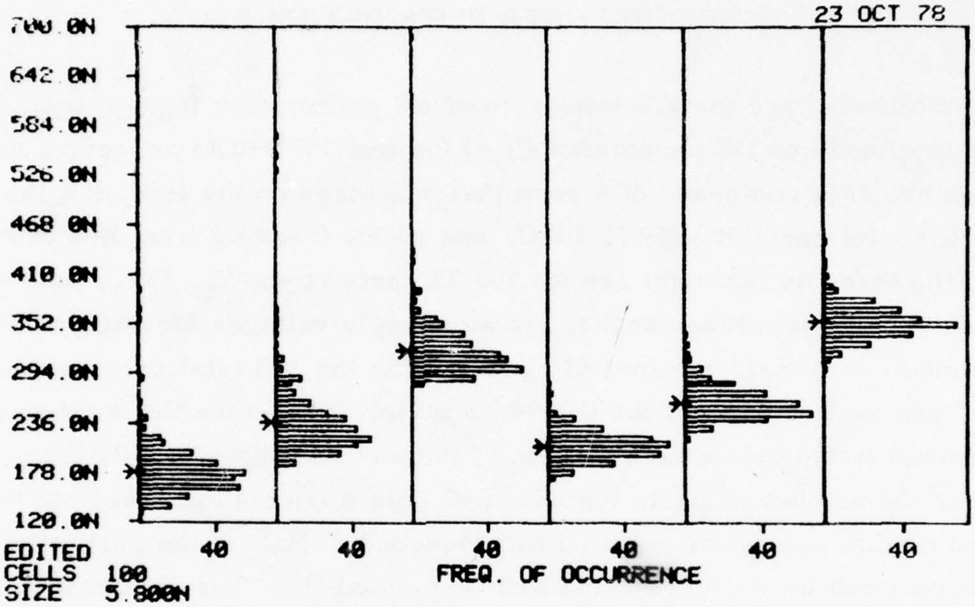
BIT MAP FOR TI TMS2708 UV-PROM

A0							1	0	1	0	1	0	1	0	1	1	1	0	0	0	1	0
A1							0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
A2							0	0	0	0	1	1	1	1	1	1	0	0	1	1	0	0
A3							0	0	1	1	0	0	1	1	0	1	0	0	0	1	1	1
	A9	A8	A7	A6	A5	A4	1	0	9	8	5	4	13	12	7	15	3	2	6	14	11	10
48	1	1	0	0	0	0																
16	0	1	0	0	0	0																
32	1	0	0	0	0	0																
0	0	0	0	0	0	0																
56	1	1	1	0	0	0																
24	0	1	1	0	0	0																
40	1	0	1	0	0	0																
8	0	0	1	0	0	0																
52	1	1	0	1	0	0																
20	0	1	0	1	0	0																
36	1	0	0	1	0	0																
4	0	0	0	1	0	0																
60	1	1	1	1	0	0																
28	0	1	1	1	0	0																
44	1	0	1	1	0	0																
12	0	0	1	1	0	0																
50	1	1	0	0	1	0																
18	0	1	0	0	1	0																
34	1	0	0	0	1	0																
2	0	0	0	0	1	0																
58	1	1	1	0	1	0																
26	0	1	1	0	1	0																
42	1	0	1	0	1	0																
10	0	0	1	0	1	0																
54	1	1	0	1	1	0																
22	0	1	0	1	1	0																
38	1	0	0	1	1	0																
6	0	0	0	1	1	0																
62	1	1	1	1	1	0																
30	0	1	1	1	1	0																
46	1	0	1	1	1	0																
14	0	0	1	1	1	0																
49	1	1	0	0	0	1																
17	0	1	0	0	0	1																
33	1	0	0	0	0	1																
1	0	0	0	0	0	1																
57	1	1	1	0	0	1																
25	0	1	1	0	0	1																
41	1	0	1	0	0	1																
9	0	0	1	0	0	1																
53	1	1	0	1	0	1																
21	0	1	0	1	0	1																
37	1	0	0	1	0	1																
5	0	0	0	1	0	1																
61	1	1	1	1	0	1																
29	0	1	1	1	0	1																
45	1	0	1	1	0	1																
13	0	0	1	1	0	1																
51	1	1	0	0	1	1																
19	0	1	0	0	1	1																
35	1	0	0	0	1	1																
3	0	0	0	0	1	1																
59	1	1	1	0	1	1																
27	0	1	1	0	1	1																
43	1	0	1	0	1	1																
11	0	0	1	0	1	1																
55	1	1	0	1	1	1																
23	0	1	0	1	1	1																
39	1	0	0	1	1	1																
7	0	0	0	1	1	1																
63	1	1	1	1	1	1																
31	0	1	1	1	1	1																
47	1	0	1	1	1	1																
15	0	0	1	1	1	1																

APPENDIX D
SCREENING DATA DISTRIBUTION PLOTS

Following are distribution plots of AC parameters (t_{ACC}, t_{OH}, and $t_{\overline{CO}}$) and one DC parameter (I_{DD}) for the UV-PROM screening tests. Each graph is composed of 6 sections: the three on the left show the data for the Intel parts at -55°C, 25°C, and 100°C (reading from left to right) and the three on the right are for the TI parts at -55°C, 25°C, and 125°C. In each plot, data taken at three power supply voltages for each part are included: nominal, nominal ±10 percent for the 103 Intel parts and nominal, nominal ±5 percent for the 94 TI parts. Therefore the number of readings listed below each section of the plot is approximately three times the number of parts tested. (AC data were not recorded for any reading that was greater than 1 microsecond.) Half of the parts were programmed by method P1 and half by method P2. The abscissa of each bar on the plots is the number of readings for which the value of the parameter indicated by the ordinate of each bar was observed. The units of the ordinates are nanoseconds for the timing parameters and milliamperes for I_{DD}. The mean value of each population is indicated by an arrow on each plot and is listed below the plot, together with other statistical parameters.

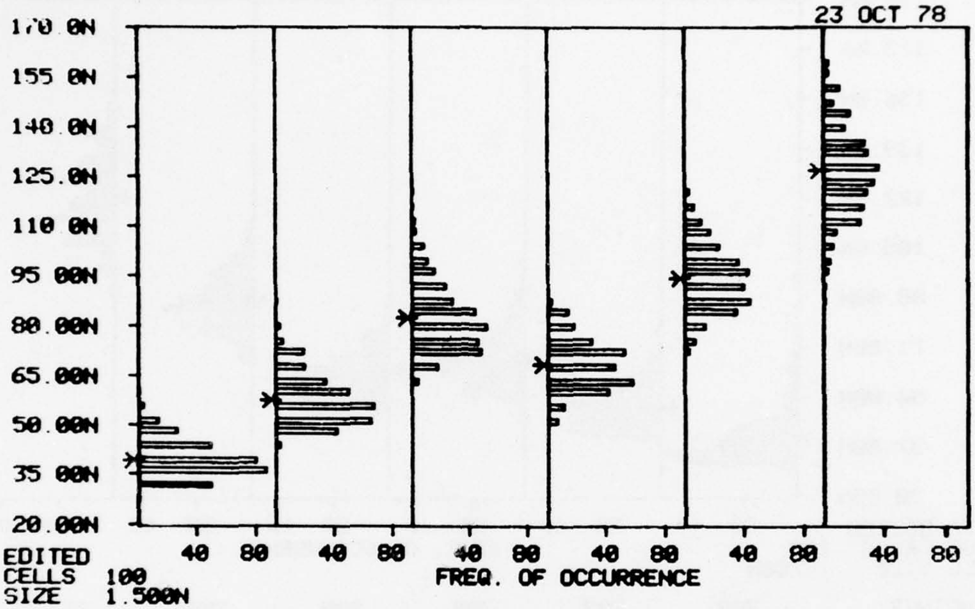
```
S-3260     DATA FOR TACC          INT........SCREEN............TEX
```



```
DATA EDITED
# OF CELLS   100
CELL SIZE    5.800N

READINGS:        309        309        301        280        282        279
MAXIMUM:      390.0N     570.0N     690.0N     280.0N     340.0N     450.0N
MEAN:         180.4N     237.9N     321.1N     210.5N     260.6N     355.5N
MINIMUM:      130.0N     190.0N     280.0N     170.0N     220.0N     300.0N
STD DEV :     30.81N     43.86N     33.15N     17.66N     19.89N     20.32N
```

```
S-3260     DATA FOR TOH           INT........SCREEN............TEX
```



```
DATA EDITED
# OF CELLS   100
CELL SIZE    1.500N

READINGS:        309       309       305       288       282       279
MAXIMUM:       60.00N    88.00N    120.0N    88.00N    120.0N    160.0N
MEAN:          39.60N    57.90N    82.36N    68.49N    94.34N    126.8N
MINIMUM:       28.00N    44.00N    64.00N    52.00N    72.00N    88.00N
STD.DEV.:      5.730N    7.753N    10.25N    7.671N    9.850N    13.37N
```

S-3260 DATA FOR TCO INT........SCREEN............TEX

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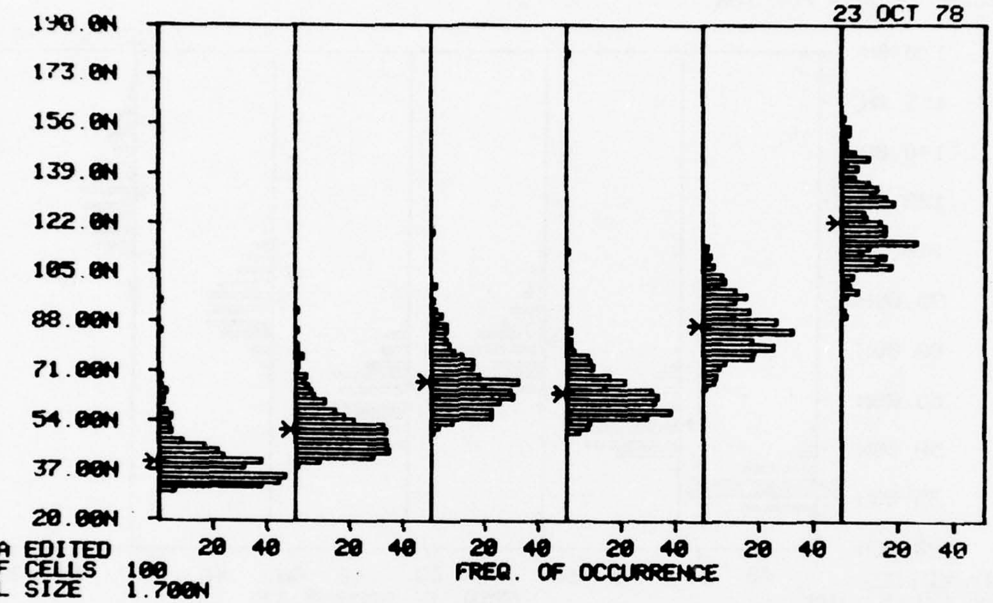
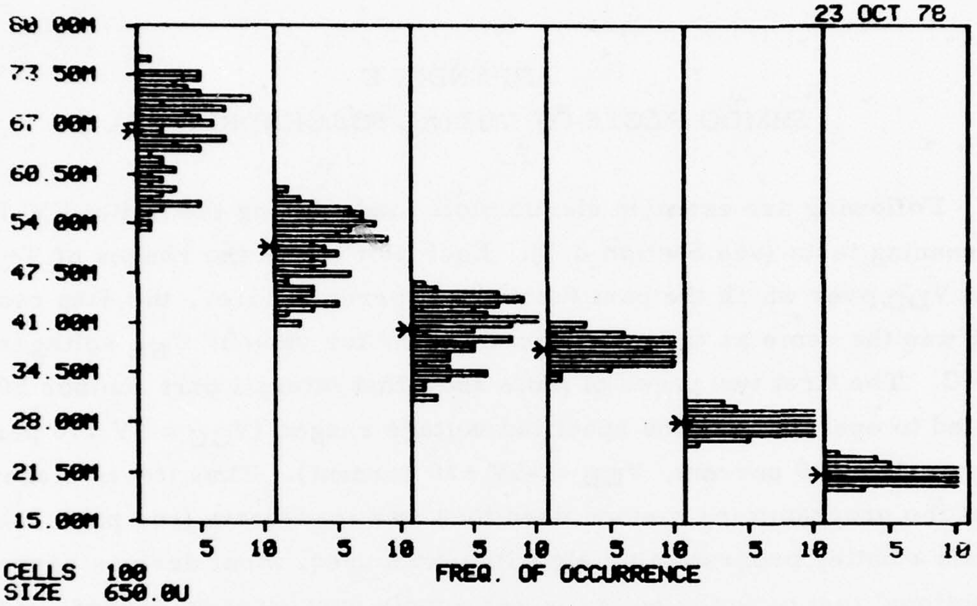


```
DATA EDITED
# OF CELLS   100
CELL SIZE    1.700N

READINGS:        309       309       306       280       282       282
MAXIMUM:      94.00N    92.00N    118.0N    180.0N    114.0N    158.0N
MEAN:         40.03N    51.24N    67.45N    63.51N    86.79N    122.2N
MINIMUM:      30.00N    38.00N    50.00N    50.00N    66.00N    90.00N
STD.DEV.:     8.259N    8.312N    9.729N    10.10N    9.679N    13.59N
```

```
3-3260    DATA FOR IDD          INT........SCREEN.............TEX
```



```
# OF CELLS   100
CELL SIZE    650.0U

READINGS:       103       103       103        94        94        94
MAXIMUM:     75.63M    58.47M    46.15M    40.82M    30.50M    23.87M
MEAN:        65.99M    50.85M    40.22M    37.59M    28.06M    21.40M
MINIMUM:     53.19M    40.69M    31.25M    33.79M    25.68M    19.63M
STD.DEV.:    5.439M    4.378M    3.642M    1.545M    1.095M    937.7U
```

APPENDIX E
SHMOO PLOTS OF INITIAL SCREENING DATA

Following are example shmoo plots made during the initial UV-PROM screening tests (see Section 2. 2). Each plot shows the ranges of V_{CC} and V_{DD} over which the part functioned correctly, i. e., the data read out was the same as the programmed data, for various V_{BB} voltages at 25°C. The first two pages of plots show that Intersil part number 503 failed to operate over the specified voltage ranges (V_{CC} = 5V ±10 percent, V_{DD} = 12V ±10 percent, V_{BB} = -5V ±10 percent). Thus it was discovered that the programming method used then was inadequate (see page 13). When a better programming algorithm was used, most devices passed the functional test over the entire power supply specification ranges. Example shmoo plots for a good device, TI number 13, are also included in this appendix.

```
 UV PROM   VCC VS VDD  WITH VBB CONSTANT  TEMP:   25     SN:  503
(*) DENOTES PASS FUNCTIONAL                         DATE:07 OCT 77

VCC(V)        VBB(V)= -3.00
 3.00  *********
 3.50 ****************
 4.00 *********************
 4.50 ****************************
 5.00 *******************************
 5.50 *******************************
 6.00 *******************************
 6.50 *******************************
 7.00 *******************************
 7.50 *******************************
 8.00 *******************************
 8.50 *******************************
 9.00 *******************************
 9.50 *******************************
      ^....^....^....^....^....^....^
VDD=  8    9    10   11   12   13   14 VOLTS

VCC(V)        VBB(V)= -3.50
 3.00 **********
 3.50 ****************
 4.00 ******************** *
 4.50 **************************
 5.00 *******************************
 5.50 *******************************
 6.00 *******************************
 6.50 *******************************
 7.00 *******************************
 7.50 *******************************
 8.00 *******************************
 8.50 ***************************
 9.00 ***************************
 9.50 ***************************
      ^....^....^....^....^....^....^
VDD=  8    9    10   11   12   13   14 VOLTS

VCC(V)        VBB(V)= -4.00
 3.00 **********
 3.50 ****************
 4.00 ******************** *
 4.50 ************************** *
 5.00 *******************************.
 5.50 *******************************
 6.00 *******************************
 6.50 ******************************
 7.00 *******************
 7.50 *******************
 8.00 *********************
 8.50 **********************
 9.00 **********************
 9.50 **********************
      ^....^....^....^....^....^....^
VDD=  8    9    10   11   12   13   14 VOLTS
```

```
VCC(V)      VBB(V)= -4.50
 3.00 **********
 3.50 ****************
 4.00 *********************
 4.50 ***********************
 5.00 ************************
 5.50 **********************
 6.00 *************
 6.50 **************
 7.00 **************
 7.50 **************
 8.00 **************
 8.50 *************
 9.00 *************
 9.50 ************
      ^....^....^....^....^....^....^
VDD=  8    9    10   11   12   13   14 VOLTS

VCC(V)      VBB(V)= -5.00
 3.00 **********
 3.50 **************
 4.00 ***************
 4.50 **************
 5.00 *********
 5.50 *********
 6.00 *********
 6.50 *********
 7.00 *********
 7.50 *********
 8.00 ********
 8.50 ********
 9.00 *******
 9.50 *******
      ^....^....^....^....^....^....^
VDD=  8    9    10   11   12   13   14 VOLTS

VCC(V)      VBB(V)= -5.50
 3.00   ******
 3.50 ********
 4.00 ****
 4.50 ****
 5.00 *****
 5.50 *****
 6.00 *****
 6.50 ****
 7.00 ****
 7.50 ****
 8.00.
 8.50
 9.00
 9.50  *
      ^....^....^....^....^....^....^
VDD=  8    9    10   11   12   13   14 VOLTS
```

```
  OV FROM    VCC VS VDD  WITH VBB CONSTANT   TEMP:    25      SN:    13
(*) DENOTES PASS FUNCTIONAL                            DATE:07 OCT 77


VCC(V)        VBB(V)= -3.00
  3.00 *
  3.50 ***************
  4.00 *******************************
  4.50 *******************************
  5.00 *******************************
  5.50 *******************************
  6.00 *******************************
  6.50 *******************************
  7.00 *******************************
  7.50 *******************************
  8.00 *******************************
  8.50 *******************************
  9.00 *******************************
  9.50 *******************************
       ^....^....^....^....^....^....^
VDD=   8    9    10   11   12   13   14 VOLTS


VCC(V)        VBB(V)= -3.50
  3.00 *******************************
  3.50 *******************************
  4.00 *******************************
  4.50 *******************************
  5.00 *******************************
  5.50 *******************************
  6.00 *******************************
  6.50 *******************************
  7.00 *******************************
  7.50 *******************************
  8.00 *******************************
  8.50 *******************************
  9.00 *******************************
  9.50 *******************************
       ^....^....^....^....^....^...:^
VDD=   8    9    10   11   12   13   14 VOLTS


VCC(V)        VBB(V)= -4.00
  3.00 *******************************
  3.50 *******************************
  4.00 *******************************
  4.50 *******************************
  5.00 *******************************
  5.50 *******************************
  6.00 *******************************
  6.50 *******************************
  7.00 *******************************
  7.50 *******************************
  8.00 *******************************
  8.50 *******************************
  9.00 *******************************
  9.50 *******************************
       ^....^....^....^....^....^....^
VDD=   8    9    10   11   12   13   14 VOLTS
```

```
VCC(V)        VBB(V)= -4.50
  3.00 *******************************
  3.50 *******************************
  4.00 *******************************
  4.50 *******************************
  5.00 *******************************
  5.50 *******************************
  6.00 *******************************
  6.50 *******************************
  7.00 *******************************
  7.50 *******************************
  8.00 *******************************
  8.50 *******************************
  9.00 *******************************
  9.50 *******************************
       ^....^....^....^....^....^....^
VDD=   8    9    10   11   12   13   14 VOLTS
```

```
VCC(V)        VBB(V)= -5.00
  3.00 *******************************
  3.50 *******************************
  4.00 *******************************
  4.50 *******************************
  5.00 *******************************
  5.50 *******************************
  6.00 *******************************
  6.50 *******************************
  7.00 *******************************
  7.50 *******************************
  8.00 *******************************
  8.50 *******************************
  9.00 *******************************
  9.50 *******************************
       ^....^....^....^....^....^....^
VDD=   8    9    10   11   12   13   14 VOLTS
```

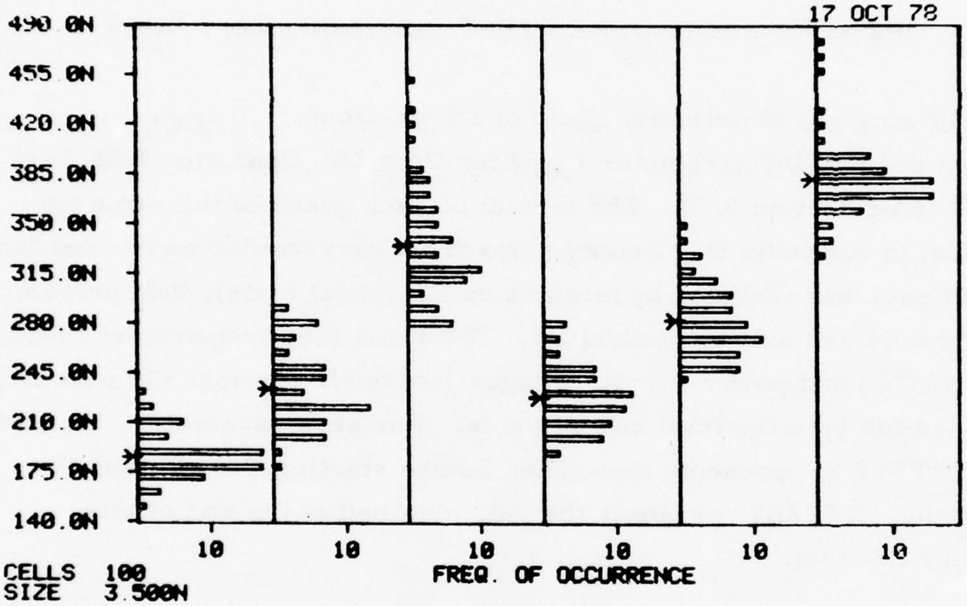
```
VCC(V)        VBB(V)= -5.50
  3.00 *******************************
  3.50 *******************************
  4.00 *******************************
  4.50 *******************************
  5.00 *******************************
  5.50 *******************************
  6.00 *******************************
  6.50 *******************************
  7.00 *******************************
  7.50 *******************************
  8.00 *******************************
  8.50 *******************************
  9.00 *********************** *******
  9.50 **********************
       ^....^....^....^....^....^....^
VDD=   8    9    10   11   12   13   14 VOLTS
```

APPENDIX F

OPTIMUM PROCEDURES TEST DISTRIBUTION PLOTS

Following are distribution plots of AC parameters (t_{ACC}, t_{OH}, and $t_{\overline{CO}}$) and one DC parameter (I_{DD}) for Test 2B, Operating Life Test at 125°C (see Section 5. 2). The format of each graph is the same as described in Appendix D. Twenty parts from each vendor were used (an extra TI part was included by mistake on the initial tests), half programmed by method P1 and half by method P2. The same test temperatures (-55, 25 and 125°C) and power supply voltages (nominal, nominal ±10 percent) were used for both the Intel and TI parts. For each parameter, the plot labeled "TST2B0" presents data taken before starting Test 2B and the plot labeled "TST2B7" presents the data obtained at the end of this 1000 hour life test.

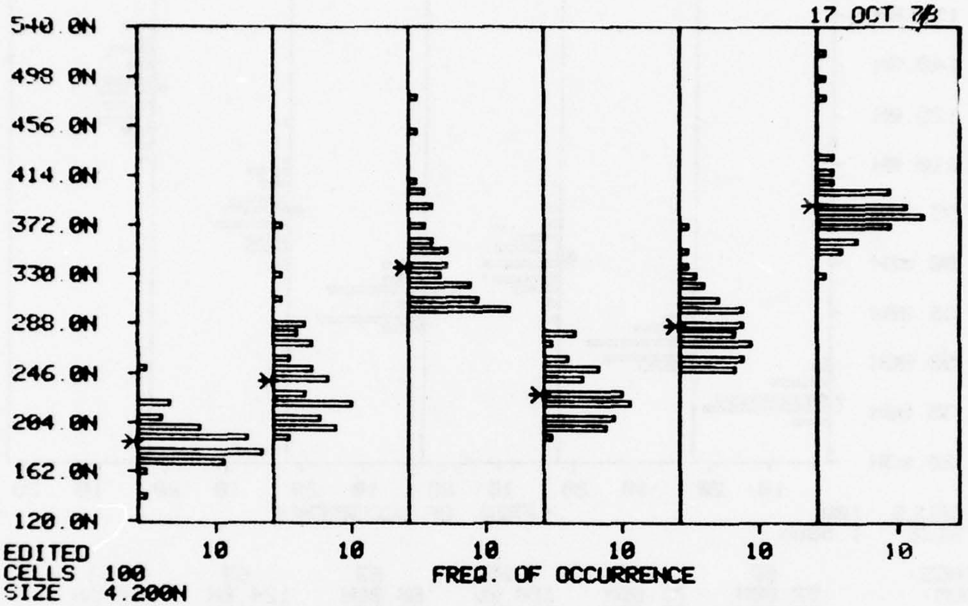
```
S-3260     DATA FOR TACC          INT........TST2B0............TEX
```



```
# OF CELLS   100
CELL SIZE    3.500N

READINGS:          60        60        60        63        63        63
MAXIMUM:       230.0N    290.0N    450.0N    280.0N    350.0N    480.0N
MEAN:          186.3N    234.0N    334.3N    228.3N    282.7N    382.5N
MINIMUM:       150.0N    180.0N    280.0N    190.0N    240.0N    330.0N
STD DEV.:      15.94N    27.87N    39.16N    22.33N    25.35N    26.70N
```

```
S-3260    DATA FOR TACC              INT........TST2B7............TEX
```

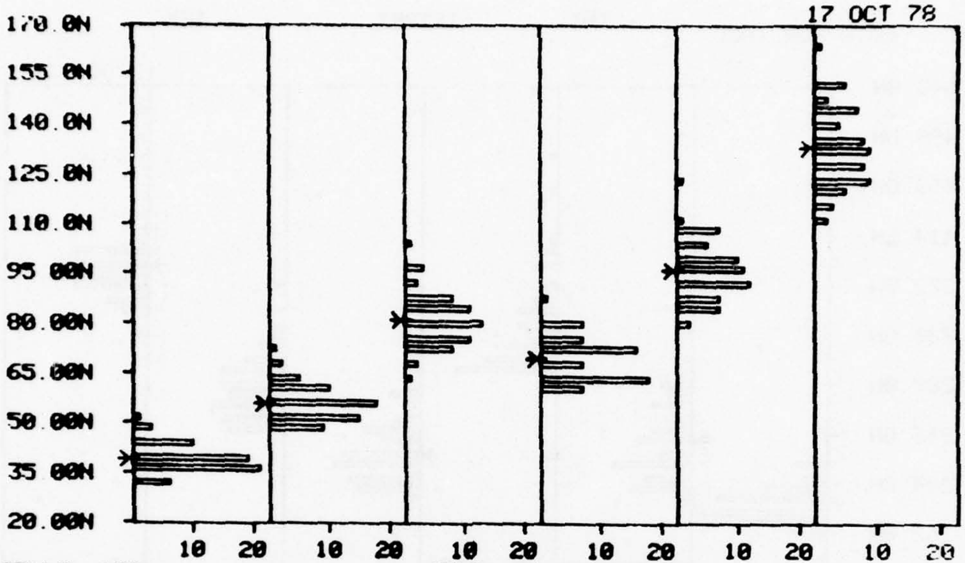


```
DATA EDITED
# OF CELLS  100
CELL SIZE  4.200N

READINGS:        59        59        57        59        60        60
MAXIMUM:     250.0N    370.0N    480.0N    280.0N    370.0N    520.0N
MEAN:        187.6N    240.2N    336.0N    229.2N    286.2N    389.3N
MINIMUM:     140.0N    190.0N    300.0N    190.0N    250.0N    330.0N
STD.DEV.:    17.75N    36.70N    39.28N    23.14N    27.00N    32.31N
```

S-3260 DATA FOR TOH INT.........TST2B0.............TEX

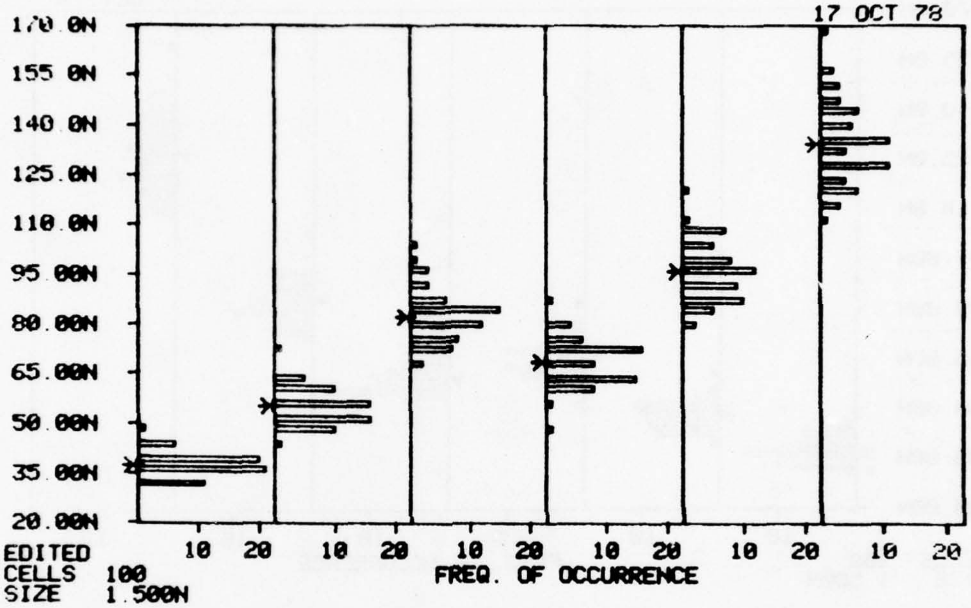
17 OCT 78



```
# OF CELLS  100
CELL SIZE   1.500N

READINGS:        60       60       60       63       63       63
MAXIMUM:     52.00N   72.00N   104.0N   88.00N   124.0N   164.0N
MEAN:        39.07N   55.80N   80.93N   69.52N   95.81N   133.0N
MINIMUM:     32.00N   48.00N   64.00N   60.00N   80.00N   112.0N
STD.DEV.:    4.441N   5.581N   7.702N   6.602N   8.694N   11.26N
```

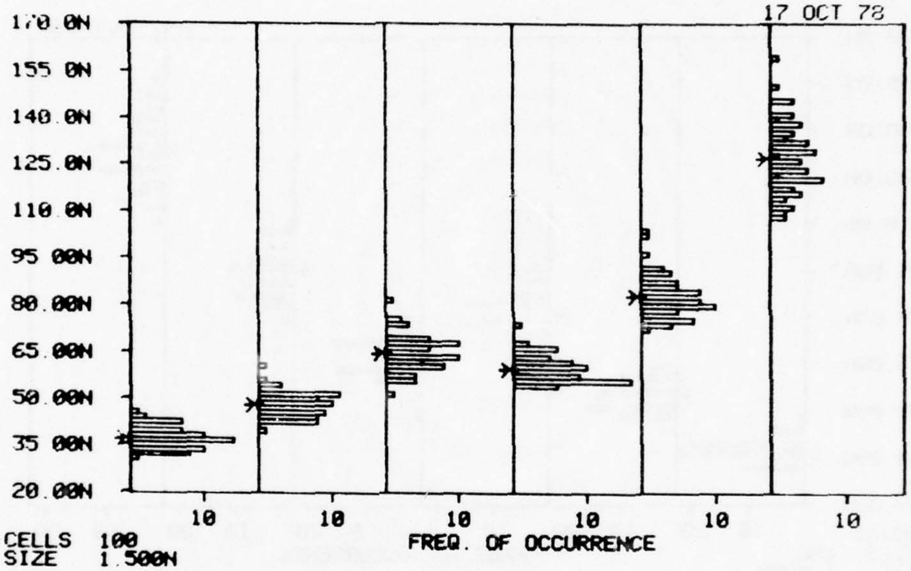
```
S-3260     DATA FOR TOH          INT........TST2B7............TEX
```



```
DATA EDITED
# OF CELLS    100
CELL SIZE     1.500N

READINGS:            59        59        58        60        60        60
MAXIMUM:          48.00N    72.00N    104.0N    88.00N    120.0N    168.0N
MEAN:             37.63N    54.98N    82.14N    68.40N    95.80N    134.2N
MINIMUM:          32.00N    44.00N    68.00N    48.00N    80.00N    112.0N
STD.DEV. :        3.868N    5.438N    7.722N    7.014N    8.539N    11.61N
```

```
S-3260     DATA FOR TCO            INT........TST2B0............TEX
                                                              17 OCT 78
```

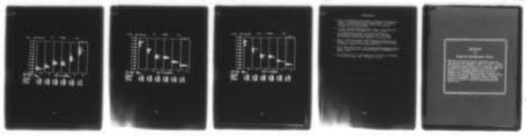


```
# OF CELLS   100
CELL SIZE    1.500N

READINGS:           60        60        60        63        63        63
MAXIMUM:        46.00N    60.00N    82.00N    74.00N    104.0N    160.0N
MEAN:           36.97N    47.87N    64.83N    59.75N    82.95N    127.2N
MINIMUM:        30.00N    40.00N    52.00N    54.00N    72.00N    108.0N
STD.DEV.:       3.636N    4.197N    5.767N    4.318N    6.475N    11.36N
```

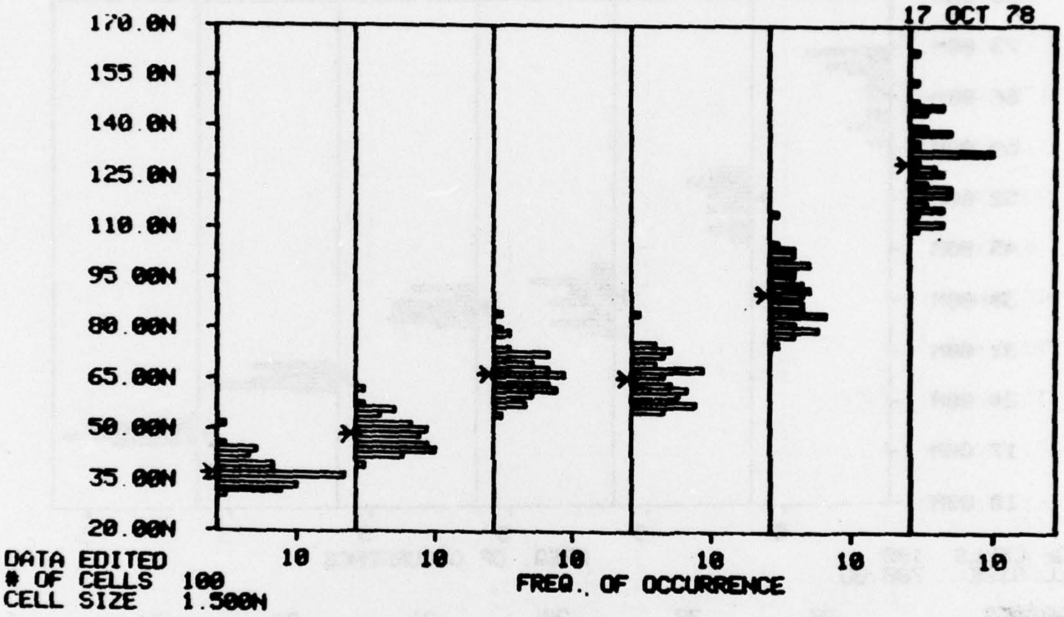
AD-A071 152 HUGHES AIRCRAFT CO CULVER CITY CA TECHNOLOGY SUPPORT DIV F/G 14/4
RELIABILITY EVALUATION OF PROGRAMMABLE READ-ONLY MEMORIES (PROM--ETC(U)
MAY 78 A P ARQUERO, R L BARCH, M B COLLIGAN F30602-75-C-0294
UNCLASSIFIED HAC-P78-341R-PT-3 RADC-TR-79-92-PT-3

2 OF 2
AD
A071152



END
DATE
FILMED
8--79
DDC

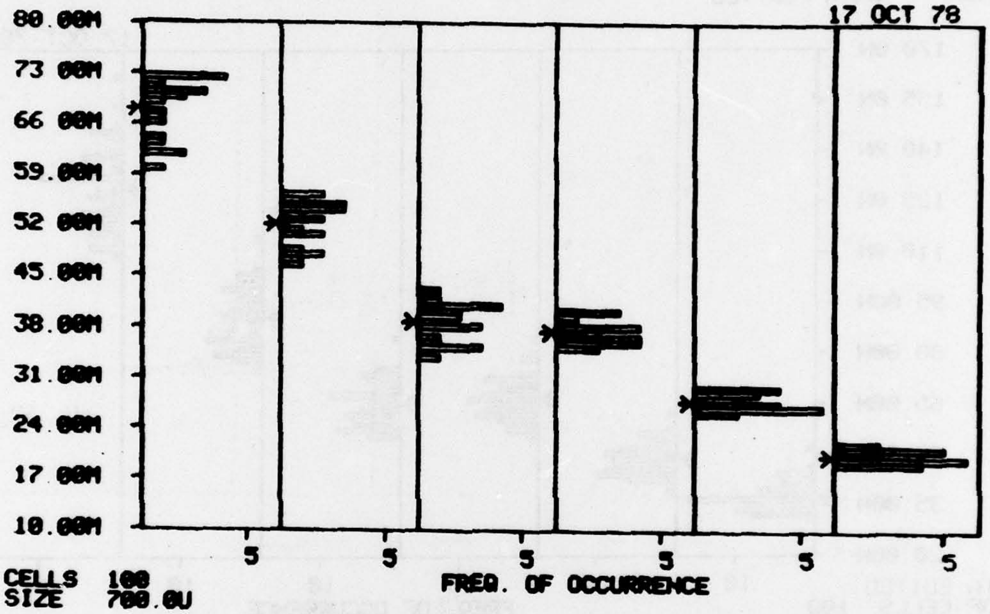
```
S-3260    DATA FOR TCO            INT........TST287............TEX
```



```
DATA EDITED
# OF CELLS  100
CELL SIZE   1.500N

READINGS:       60       60       59       59       60       60
MAXIMUM:    52.00N   62.00N   84.00N   84.00N   114.0N   162.0N
MEAN:       37.23N   48.43N   66.47N   65.39N   90.60N   129.1N
MINIMUM:    30.00N   40.00N   54.00N   56.00N   76.00N   110.0N
STD DEV.:   4.264N   4.760N   5.900N   6.447N   8.702N   11.57N
```

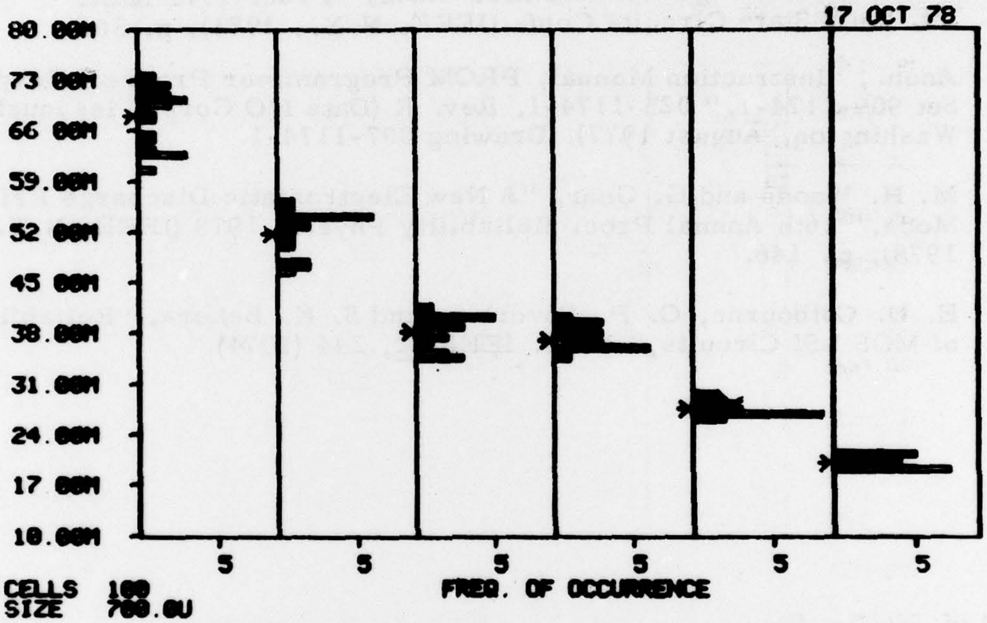
```
S-3260    DATA FOR IDD         INT........TST200............TEX
```



```
# OF CELLS   100
CELL SIZE    700.0U

READINGS:          20         20         20         21         21         21
MAXIMUM:       72.16M     56.09M     42.07M     40.20M     29.71M     21.69M
MEAN:          68.00M     52.12M     38.73M     37.45M     27.83M     20.29M
MINIMUM:       60.01M     46.45M     33.81M     35.04M     26.20M     19.06M
STD.DEV.:      3.976M     3.100M     2.673M     1.623M     1.154M     809.1U
```

```
S-3260     DATA FOR IDD          INT.....TST2B7......TEX
                                                   17 OCT 78
```



```
# OF CELLS   100
CELL SIZE    700.0U

READINGS:          20        20        20        20        20        20
MAXIMUM:       73.66M    56.07M    41.00M    39.70M    29.63M    21.30M
MEAN:          67.92M    51.70M    38.05M    37.05M    27.59M    20.05M
MINIMUM:       60.66M    46.64M    34.30M    34.82M    26.04M    18.81M
STD.DEV.:      3.991M    3.000M    2.331M    1.509M    1.127M    807.4U
```

REFERENCES

1. Anon., "Standard Electronic Modules, Exploratory Development Program, Large Function Module Testing Task, FY-77 Final Report," (Naval Weapons Support Center, Crane, Indiana, 30 September 1977), Section VIII.
2. G. Gear, "FAMOS PROM Reliability Studies," 14th Annual Proc. Reliability Physics 1976 (IEEE, N.Y., 1976), p. 198.
3. D. Frohman-Bentchkowsky, "A Fully-Decoded 2048-Bit Electrically-Programmable MOS-ROM," Proc. 1971 IEEE Int. Solid State Circuits Conf. (IEEE, N.Y., 1971), p. 80.
4. Anon., "Instruction Manual, PROM Programmer Program Card Set 909-1174-1," 025-1174-1, Rev. R (Data I/O Corp., Issaquah, Washington, August 1977), Drawing 007-1174-1.
5. M. H. Woods and G. Gear, "A New Electrostatic Discharge Failure Mode," 16th Annual Proc. Reliability Physics 1978 (IEEE, N.Y., 1978), p. 146.
6. E. D. Colbourne, G. P. Coverley, and S. K. Behera, "Reliability of MOS LSI Circuits," Proc. IEEE 62, 244 (1974).

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